PAG7920J3: Ultra-Low Power (ULP) Global Shutter Cube Camera Module

General Description

The PAG7920J3 is a reflow-compatible cubic sensor module featuring an integrated lens set and incorporating the PAG7920LT, a monochrome, ultra-low-power global shutter image sensor. It supports a resolution of 320 x 240 and image capture capability of up to 180 frame-per-second (fps).

The PAG7920J3 integrates PixArt's proprietary motion detection algorithm and low-power architecture design. This low-power architecture enables the always-on feature on the customer's applications, especially benefiting the battery-powered system. The PAG7920J3 is especially well-suited for consumer devices requiring miniaturized designs, including machine vision, surveillance-related applications such as augmented reality (AR), virtual reality (VR), AI classification & recognition, and barcode scanning.

PAG7920J3 registers can be accessed through the standard I^2C interface, while the image output support both 8-bit raw parallel output and SPI serial interface.

Key Features

- Small Form Factor
- Motion detection
- Supports LED strobe
- Auto Black Cancellation (ABC)
- Auto Exposure and Gain Control
- Programmable control
  - Frame rate
  - Mirror & Flip, WOI
- Supports multi-sensor frame sync
- Supports I^2C multi-slave ID by I/O strapping
- Data format: 8-bit RAW

Applications

- Computer vision
- Motion / Scene Change Detection
- Surveillance system

Key Parameters

Parameter	Typical Value
Array Size	320 x 240
Pixel Size	3.0 µm x 3.0 µm
Shutter Type	Global Shutter
Field of View (typ.)	71.34° (Horizontal) 53.72° (Vertical)
Max. Frame Rate	180 FPS
Signal to Noise Ratio, SNR Max	36 dB
Dynamic Range	64 dB
Sensitivity	2.968 V/Lux-sec @ 550nm
Supply Voltage	VDDMA: 3.3V VDDIO: Typ. 3.3V/1.8V/1.2V
Power Consumption	Typ. 0.76 mW (320 x 240@15FPS) Typ. 8.54 mW (320 x 240@180FPS) <100 µW (motion detection state)
Operating Temperature, T_J	-30 to +70 °C
Stable image, T_J	0 to +50 °C
Module Type	Cubic form factor (sensor + lens set only)
Module Dimension (L x W x H)	2.94 x 2.44 x 2.11 mm^3
Module Weight	Typ. 22.8mg

Ordering Information

Part Number	Description	Package Type	Packing Type	MOQ
PAG7920J3	Ultra-Low Power (ULP) Global Shutter Cubic Sensor Module	-	Tray	4500

RoHS compliant

For any additional inquiries, please contact us at https://www.pixart.com

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1.0 Introduction

1.1 Overview

The PAG7920J3 is a QVGA CMOS cubic sensor module integrating the image sensor PAG7920LT with a 320 x 240 active imaging pixel array. It is a global shutter module designed for fast-moving object image applications.

The PAG7920J3 supports the motion detection function that adopts the frame-based difference to detect motion events within a configurable image area. It supports programmable controls for frame rate, mirror/flip and WOI.

The image data can be transmitted via the Parallel or SPI interface, while the control command uses the I^2C interface.

Note: Throughout this document, the PAG7920J3 is referred to as the "module".

Figure 1. Module Top View

1.2 Block Diagram

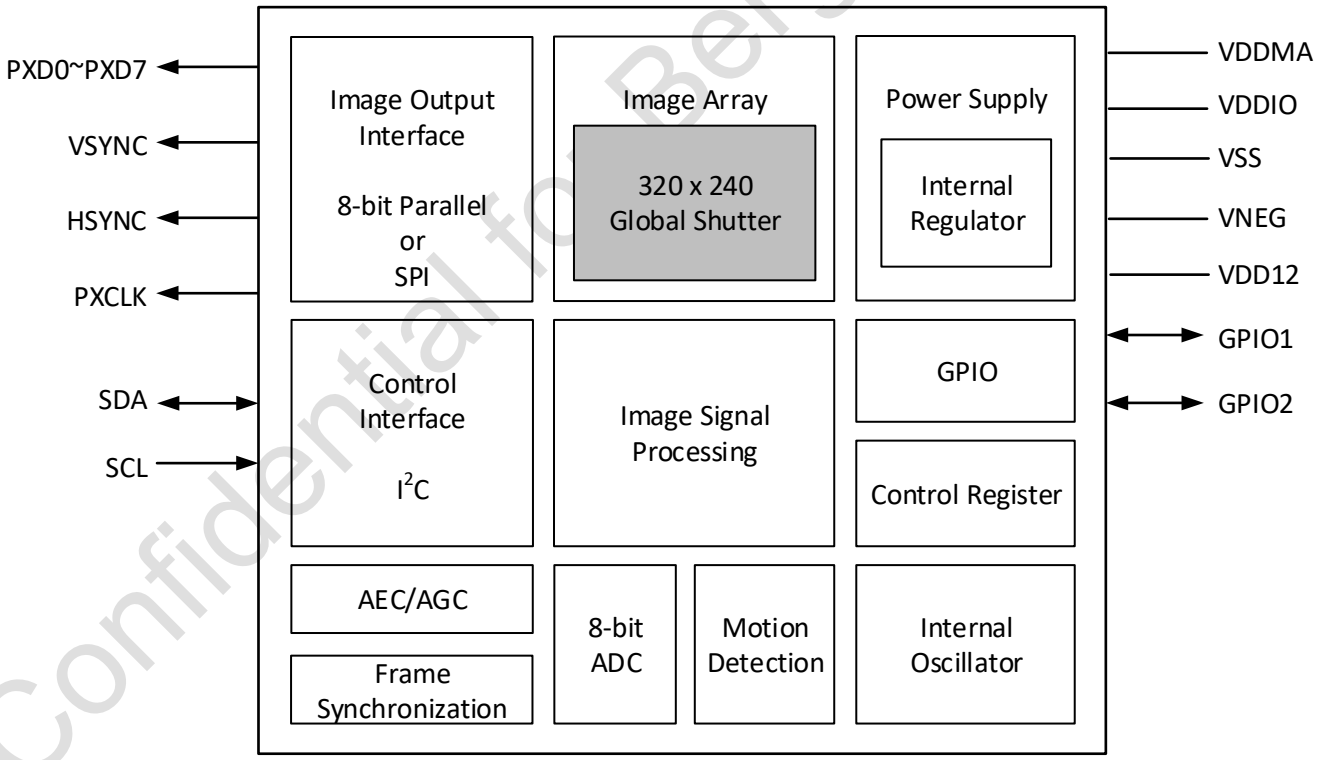


Figure 2. Image Sensor Block Diagram

1.3 Terminology

Term	Description
Min.	Minimum
Typ.	Typical
Max.	Maximum
SPI	Serial Peripheral Interface
I^2C	Inter-Integrated Circuit
WOI	Window of Interest
ULP	Ultra-Low Power
I/O	Input / Output
GPIO	General Purpose Input Output
INT	Interrupt
Sync.	Synchronization
LDO	Low-Dropout Regulator
CRA	Chief Ray Angle

1.4 Pin Assignment and Signal Description

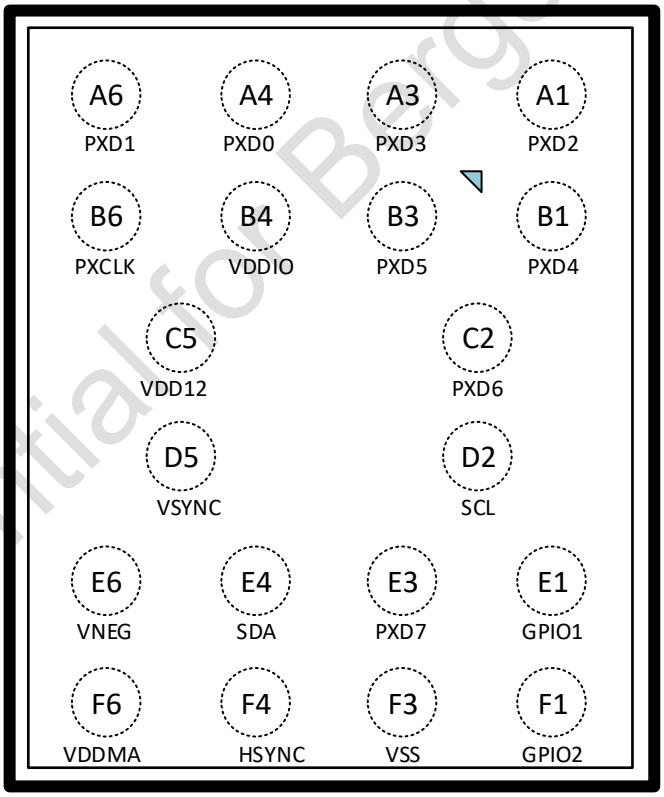


Figure 3. Pin Assignment (Bottom View)

Table 1. Signal Description

Function	Connector Pin No.	Signal Name	Type	Description
Power Supplies	F6	VDDMA	Power	Main power supply. Connects to 10µF & 0.1µF bypass capacitor.
	B4	VDDIO	Power	I/O power input. Connects to 10µF & 0.1µF bypass capacitor.
	F3	VSS	Ground	Ground
	C5	VDD12	Power	1.2V external power supply or internal regulator for core power.
	E6	VNEG	Power	Regulator output, for sensor power reference. Connects to a 1µF bypass capacitor.
Control Interface	D2	SCL	Input	I^2C clock pin (Open Drain)
	E4	SDA	I/O	I^2C data pin (Open Drain)
Image Output Interface	A4	PXD0/MISO	Output	Parallel pixel data bit[0] / SPI Master Input Slave Output
	A6	PXD1	Output	Parallel pixel data bit[1]
	A1	PXD2	Output	Parallel pixel data bit[2]
	A3	PXD3	Output	Parallel pixel data bit[3]
	B1	PXD4	Output	Parallel pixel data bit[4]
	B3	PXD5	Output	Parallel pixel data bit[5]
	C2	PXD6	Output	Parallel pixel data bit[6]
	E3	PXD7	Output	Parallel pixel data bit[7]
	F4	HSYNC/MOSI	I/O	Parallel line signal/SPI Master Output Slave Input
	D5	VSYNC/CS	I/O	Parallel frame signal/SPI Chip Select
	B6	PXCLK/SCK	I/O	Parallel pixel clock/serial clock of SPI interface
Functional I/O	E1	GPIO1	I/O	General Purpose Input Output
	F1	GPIO2	I/O	General Purpose Input Output

1.5 Pixel Map

The sensor has an image array of 320 columns by 240 rows (76800 pixels). Figure 4 shows pixel map of the image sensor array.

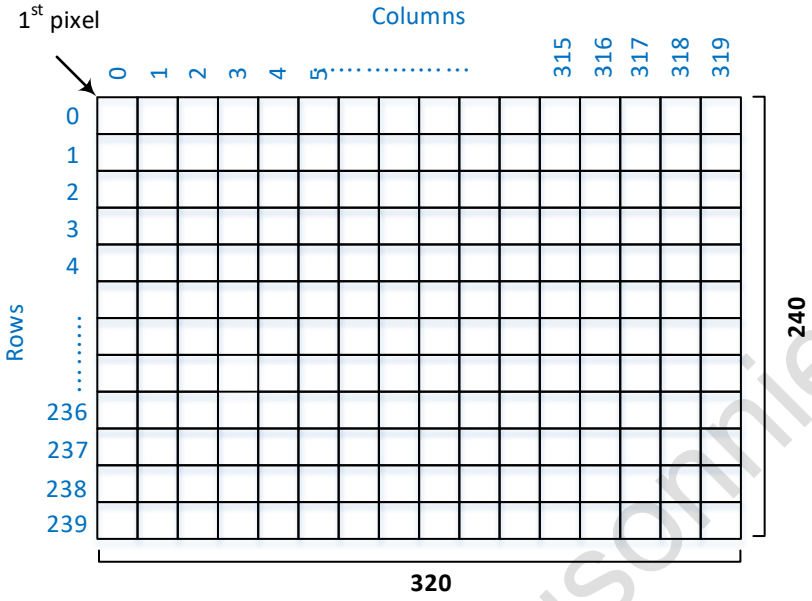


Figure 4. Sensor Array Structure

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-40	85	°C	
Main Voltage Supply	VDDMA	-0.3	4.5	V	
I/O Voltage Supply	VDDIO	-0.3	4.5	V	
Core Power Voltage Supply	VDD12	-0.3	3	V	
I/O Pin Voltage	-	-0.3	VDDIO+0.3	V	
Relative Humidity	RH	0	85	%	Non-condensing, Non-biased
Lead-free Solder Temperature	T_{SOLDER}	-	260	°C	
ESD	ESD_{HBM}	-	2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap intervals.

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature	-	-30	-	70	°C	Junction Temperature
Stable Image Temperature	-	0	-	50	°C	Junction Temperature
Main Voltage Supply	VDDMA	3.14	3.3	3.45	V	Include ripples
I/O Voltage Supply	VDDIO	1.14	1.2/1.8	3.45	V	Include ripples VDDIO ≦ VDDMA
Core Voltage Supply	VDD12	1.14	1.2	1.26	V	Include ripples
Power Ripple Noise	V_{NPP}	-	-	50	mV	Peak to peak voltage. It is applicable for VDDMA, VDDIO and VDD12.
System clock frequency	f_{sysclk}	-	24	-	MHz	Square wave Duty cycle= 45% to 55%

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 DC Electrical Characteristics

Table 4. DC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
DC Supply Current	I_{DDMA}	-	0.15	-	mA	Parallel QVGA Output at 15fps
	I_{DDIO}[2]	-	0.15	-		
	I_{DDMA}	-	1.64	-	mA	Parallel QVGA Output at 180fps
	I_{DDIO}[2]	-	1.74	-		
Motion Detect Current	I_{DDMA_MD}	-	16.2	-	µA	2fps
	I_{DDIO_MD}	-	12	-		
Suspend Current	I_{DDMA_SUS}	-	10	-	µA	
	I_{DDIO_SUS}	-	1	-		
I/O Input High Voltage	V_{IH}	0.8xVDDIO	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.4	V	VDDIO ≥ 2V
	V_{IL}	-	-	0.2xVDDIO		VDDIO < 2V
I/O Output High Voltage	V_{OH}	0.8xVDDIO	-	-	V	
I/O Output Low Voltage	V_{OL}	-	-	0.2xVDDIO	V	
Digital I/O Driving Ability	I_{DDIODR}	-	-	16	mA	VDDIO= 3.3V
		-	-	12		VDDIO= 1.8V
		-	-	6		VDDIO= 1.2V

Notes:

1. All the parameters are tested under operating conditions: VDDMA= 3.3V, VDDIO= 3.3V/1.8V/1.2V, T_A= 25°C.
2. The typical consumed current is measured without considering the external capacitive load.

2.4 AC Electrical Characteristics

Table 5. AC Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
System Clock Rise Time	t_R	-	-	5	ns	@ C_{load}= 0.5pF, Voltage Level= 10% to 90% and f_{pxclk} = 24MHz.
System Clock Fall Time	t_F	-	-	5	ns	@ C_{load}= 0.5pF, Voltage Level= 90% to 10% and f_{pxclk} = 24MHz.

Note: All the parameters are tested under operating conditions: VDDMA= 3.3V, VDDIO= 3.3V/1.8V/1.2V, T_A= 25°C.

2.5 Chip Array Specifications

Table 6. Array Specifications

Parameter	Symbol	Value	Unit	Note
Horizontal Image Array Count	-	320	pixel	
Vertical Image Array Count	-	240	pixel	
Pixel Size	-	3 x 3	μm^2	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Signal to Noise Ratio	-	36	-	-	dB	
Dynamic Range	-	64	-	-	dB	
Sensitivity	-	2.078	-	-	V/Lux-sec	@550nm
Chief Ray Angle (CRA)	-	-	-	25.83	degree	

Table 7. Chief Ray Angle (CRA) vs. Field/Image Height

Field	Image Height(mm)	Chief Ray Angle
0.0	0	0
0.1	0.06	2.89
0.2	0.12	5.77
0.3	0.18	8.61
0.4	0.24	11.39
0.5	0.30	14.09
0.6	0.36	16.7
0.7	0.42	19.19
0.8	0.48	21.56
0.9	0.54	23.77
1.0	0.6	25.83

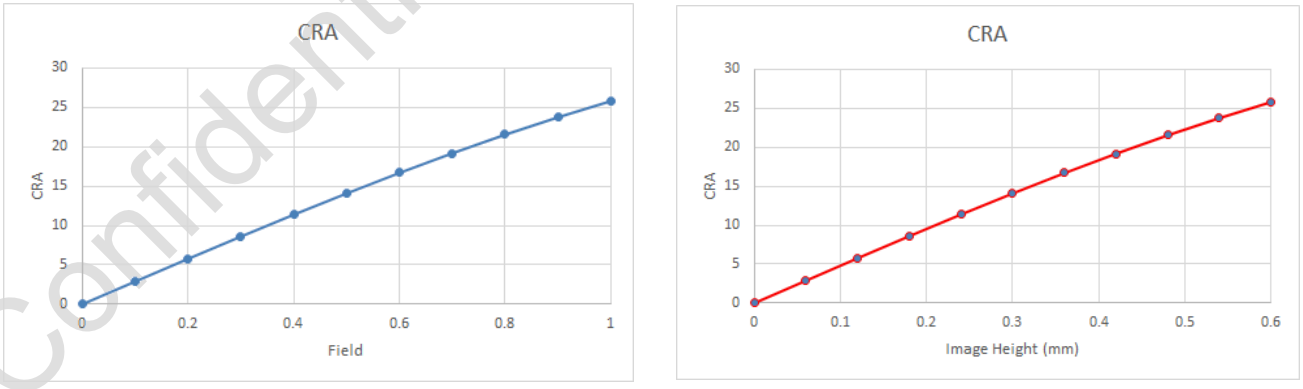


Figure 5. Chief Ray Angle (CRA) vs. Field/Image Height

2.6 Lens Typical Characteristics

Table 8. Lens Typical Characteristics

Parameter	Description	Unit	Note
Composition	1 Element	-	
Cubic Material	LCP (Black)	-	
Focus Type	Fixed Focus		
EFL	0.817	mm	
F No.	2.72	-	
Filter	No Filter		
Typical Object Distance	25mm		

2.7 Module Optical Specifications

Table 9. Optical Specifications

Parameter	Min.	Typical	Max.	Unit	Note
Field of View		71.34		degree	Horizontal
		53.72			Vertical
MTF		≥ 42		%	Center at 41 lp/mm
		≥ 42		%	0.7 Field at 41 lp/mm
Shading		≥ 30		%	0.86 Field

3.0 Mechanical Specifications

3.1 Module Mechanical Dimensions

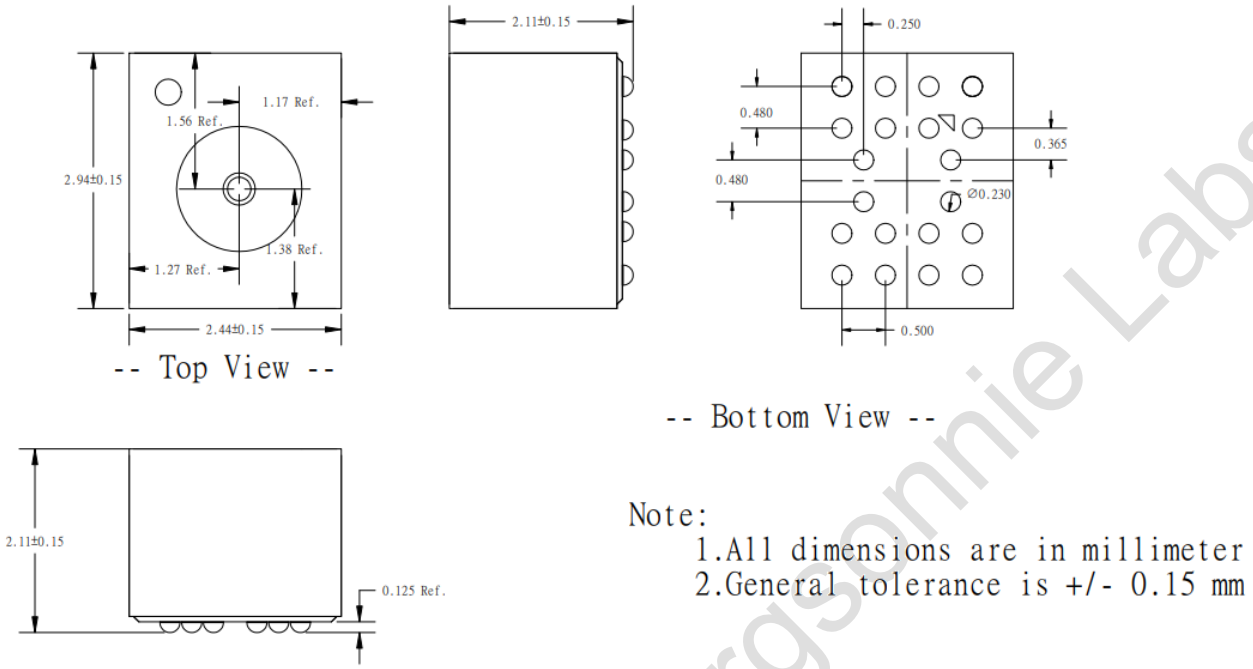


Figure 6. Module Mechanical Diagram

3.2 Module Label Identification

Table 10. Code Identification

Marking	Description
XX	Assy. Date code
YY	Assy. Tracking code (option)
ZZ	Assy. Lot code (option)

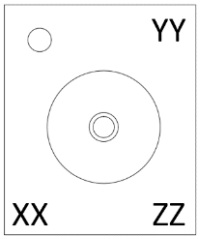


Figure 7. Package Marking

3.3 Packing Information

- Cube module Pin 1 dot orientation is toward the chamfer of chip tray, see Figure 8.
- Stack 5 trays with one cover tray in a bunch, see Figure 9.

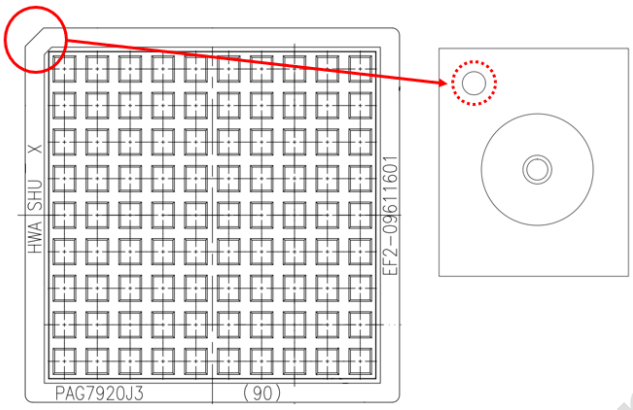


Figure 8. Module Orientation

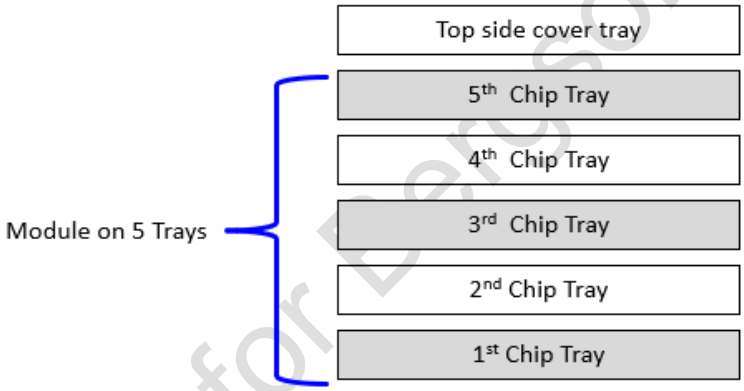


Figure 9. Stack 5+ 1 Chip Tray

- Pack 2 bunches of chip tray into one aluminum laminate moisture proof bag, see Figure 10.
- Pack 5 aluminum bags into a packing box, see Figure 11.

Figure 10. Single Bunch

Figure 11. Packing Box

Description	Value	Unit	Note
One packing box	4500	piece	(90each per tray) x (50 tray per inner box)

4.0 Design Reference

4.1 General Reference Schematic

The following schematics are the reference design for the main board, including parallel image output and SPI image output. Having LDOs generate dedicated low-noise supplies is recommended.

- For Parallel Interface:

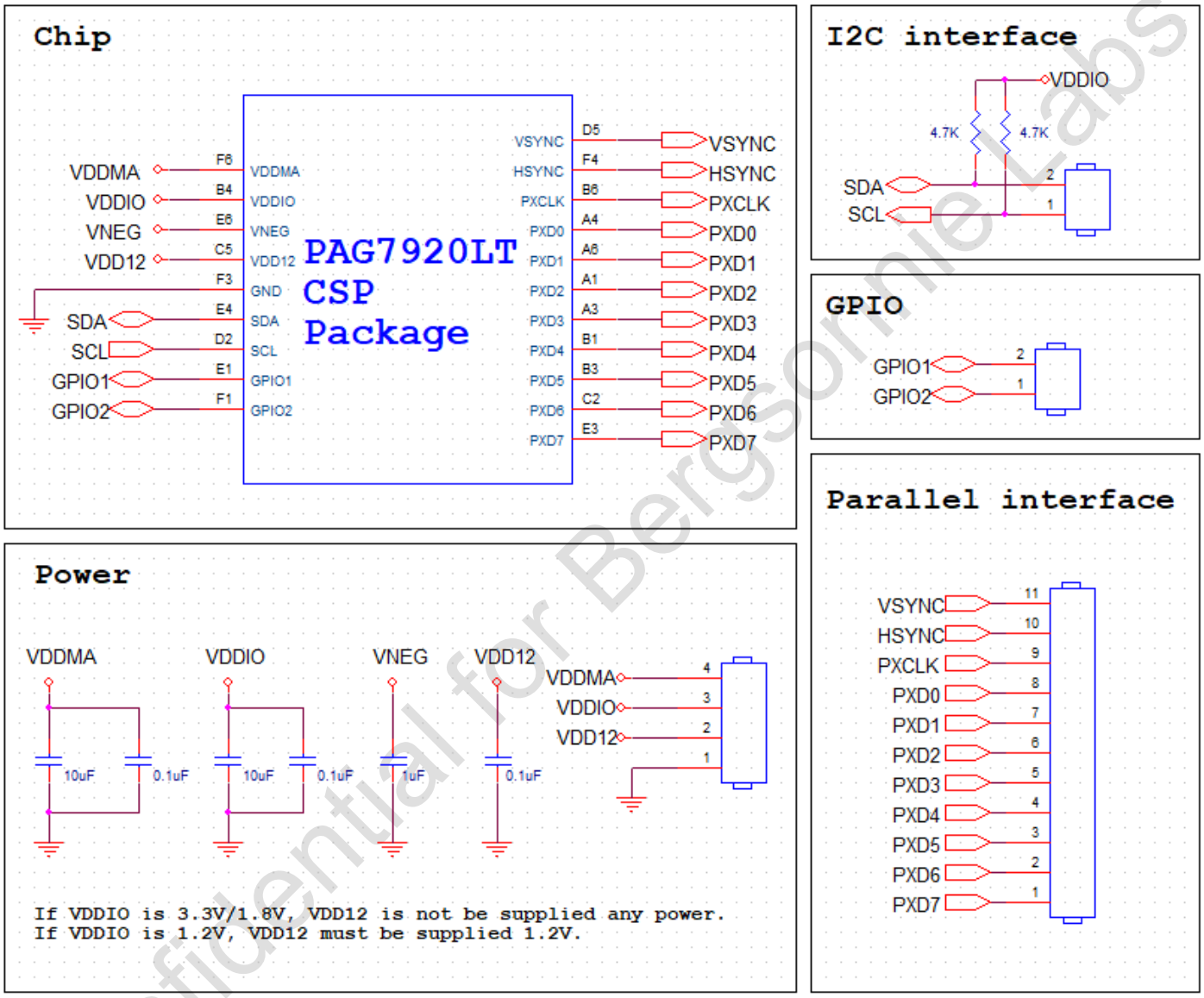


Figure 12. Reference Circuit for Image Output via Parallel Interface

- For SPI Interface:

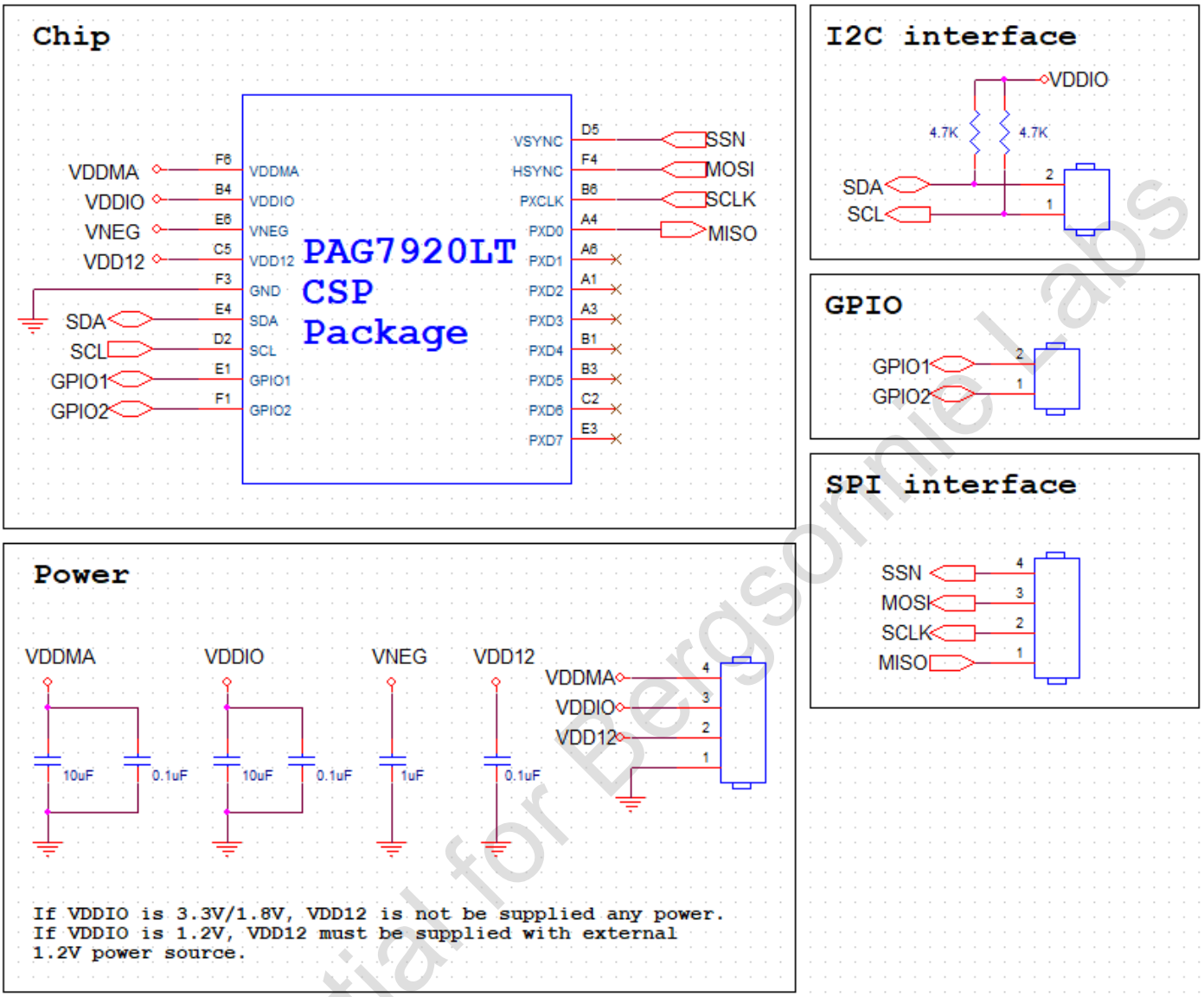


Figure 13. Reference Circuit for Image Output via SPI Interface

4.2 PCB Layout Design Guide

4.2.1 Design Rules

- Power Capacitors:
  - Place the capacitor as close as to the sensor power pin.
  - Recommended 10µF and 0.1µF power capacitors
- Pad size design:
  - If use solder mask defined (SMD), pad size is referring to solder mask opening size.
  - If use non-solder mask defined (NSMD), pad size is referring to copper metal size.

4.2.2 Recommend Footprint Dimension

Recommended dimension of pad as shown in Figure 14.

PCB pad diameter for solder ball attachment is 0.23mm.

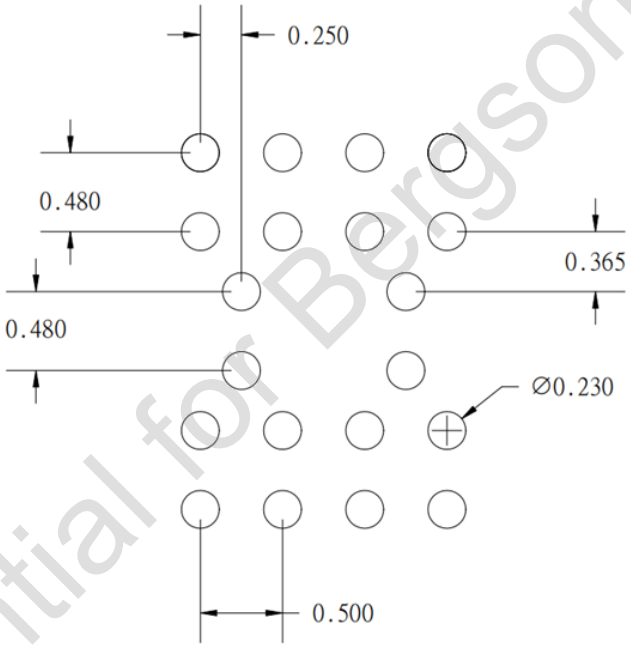


Figure 14. Recommend PCB Layout

4.3 Assembly Guide

4.3.1 IR Reflow Soldering Profile

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile as shown below.

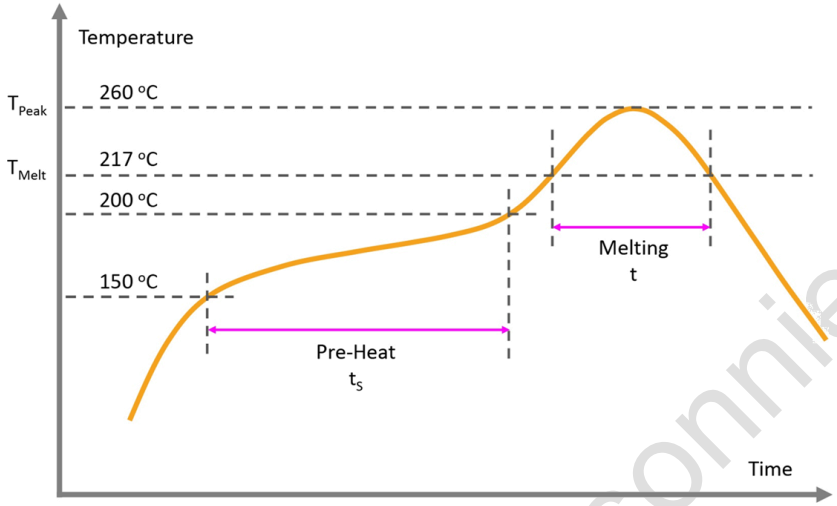


Figure 15. Reflow Profile

Table 11. Reflow Profile

Parameter	Symbol	Min.	Max.	Unit	Note
Ramp-up rate	T_{Ramp}		3	°C/sec	From T_{Melt} to T_{Peak}
Pre-heat area temperature	T_{Pre}	150	200	°C	
Pre-heat area duration	t_S	60	120	sec	
Melting duration	t	60	150	sec	
Melting Temperature	T_{Melt}	217		°C	
Peak Temperature	T_{Peak}		260	°C	

4.3.2 Under-filled Process

Epoxy under-filled process is required post Cube module mounting process as shown below.

Notes:

1. Recommend underfill supplier & type: Namics 1589-19, U8443-14
2. Unexpected failure would happen as a sequence of high temperature treatment post epoxy under-filled process, e.g. reflow.
3. Unexpected failure would happen as a sequence of improper underfill dispensing, e.g. incomplete fill

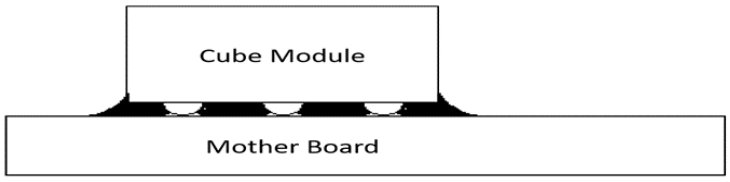


Figure 16. Epoxy Under-filled

5.0 Power Management

5.1 Regulator

The sensor consists of two integrated regulators for internal power supply. One is for VNEG and the other is for VDD12. When VDD12 is configured to use internal regulator, the VDD12 pin must be connected 0.1µF capacitor and VNEG must be connected 1µF capacitor for voltage stabilization.

5.2 VDD12

This power is for digital core power. This power pin can apply 1.2V from the external source or be configured to use the power from the internal regulator. Connects a 0.1µF bypass capacitor when configuring VDD12 to adopt the power from the internal regulator. A specific setting is required to disable the internal regulator when configuring VDD12 to apply an external 1.2V power source.

5.3 Power Sequence

Case-1: Internal Regulator for VDD12

Power-on and power-off sequence requirement as follow.

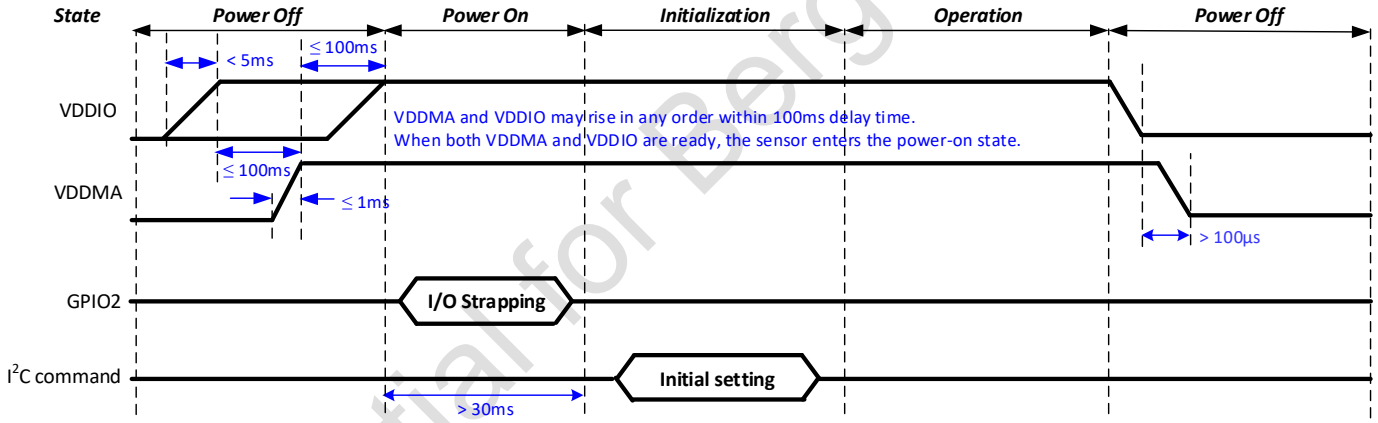


Figure 17. Power-on and Power-off Sequence

- Power-on sequence

1. VDDMA and VDDIO may rise in any order.
2. The delay time between VDDMA and VDDIO shall be within 100ms.
3. VDDIO ramp-up time must be less than 5ms.
4. VDDMA ramp-up time must be within 1ms.
5. The initialization shall start after VDDMA power on with a delay greater than 30ms (for I/O strapping).

Table 12. Internal Regulator for VDD12 Power on Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
VDDIO to VDDMA/ VDDMA to VDDIO	-	0	-	100	ms	VDDIO 90% to VDDMA 90%/ VDDMA 90% to VDDIO 90%
VDDIO Ramp-up Time	-	-	-	5	ms	VDDIO 10% to VDDIO 90%
VDDMA Ramp-up Time	-	-	-	1	ms	VDDMA 10% to VDDMA 90%
I/O Strapping duration	-	30	-	-	ms	

- Power-off Sequence

1. VDDIO must be powered off first.
2. VDDIO must be powered off prior to VDDMA with a delay greater than 100µs.

Table 13. Internal Regulator for VDD12 Power off Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
VDDIO to VDDMA timing	-	100	-	-	µs	VDDIO 10% to VDDMA 10%

Case-2: External supply for VDD12

Power-on and Power-off sequence requirement as follow.

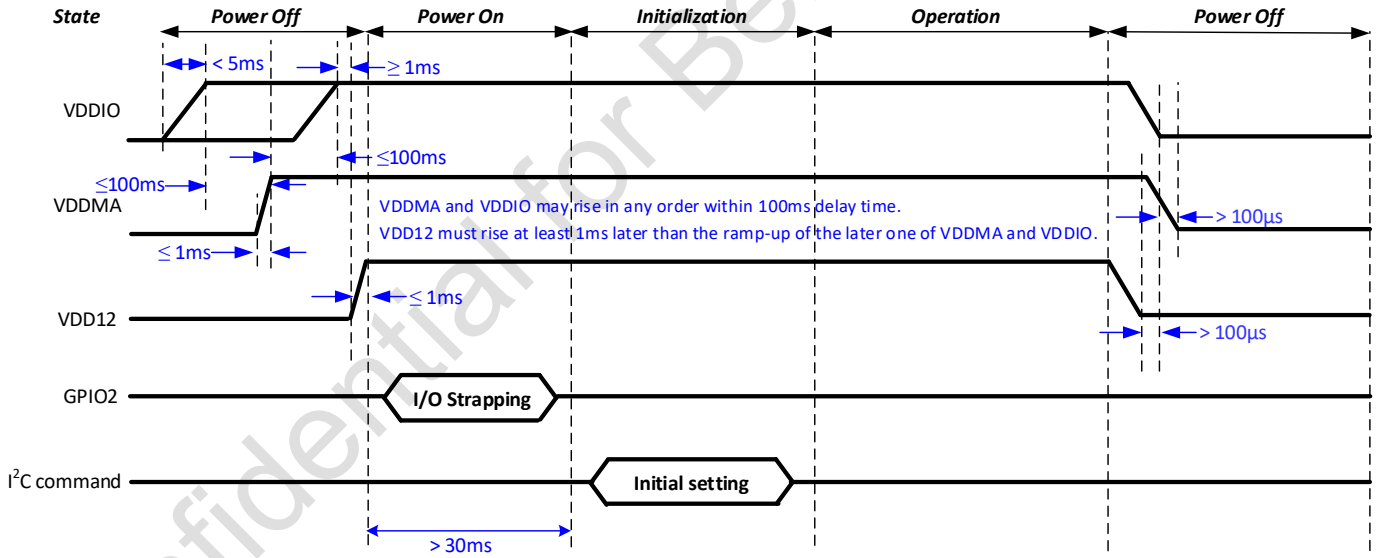


Figure 18. Power-on and Power-off Sequence

- Power-on sequence

1. VDDMA and VDDIO may rise in any order.
2. The delay time between VDDMA and VDDIO shall be within 100ms.
3. VDD12 must rise at least 1ms later than the ramp-up of the later one of VDDMA and VDDIO.
4. VDDIO ramp-up time must be less than 5ms.
5. VDDMA ramp-up time must be within 1ms.
6. VDD12 ramp-up time must be within 1ms.
7. The initialization shall start after VDD12 power on with a delay greater than 30ms (for I/O strapping).
8. Before loading initial setting, apply the below settings to disable the internal regulator for the subsequent operation,
   a. Write register 0xEF with value 0x00
   b. Write register 0x0A with value 0x37
   c. Write register 0x0B with value 0x72
   d. Write register 0x10 with value 0x01

Table 14. External Supply for VDD12 Power on Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
VDDIO to VDDMA/ VDDMA to VDDIO	-	0	-	100	ms	VDDIO 90% to VDDMA 90%/ VDDMA 90% to VDDIO 90%
VDDMA to VDD12	-	1	-	-	ms	VDDMA 90% to VDD12 90%
VDDIO Ramp-up Time	-	-	-	5	ms	VDDIO 10% to VDDIO 90%
VDDMA Ramp-up Time	-	-	-	1	ms	VDDMA 10% to VDDMA 90%
VDD12 Ramp-up Time	-	-	-	1	ms	VDD12 10% to VDD12 90%
I/O Strapping duration	-	30	-	-	ms	

- Power-off Sequence

1. VDD12 must be powered off first.
2. VDD12 must be powered off prior to VDDIO with a delay greater than 100µs.
3. VDDIO must be powered off prior to VDDMA with a delay greater than 100µs.

Table 15. Internal Regulator for VDD12- Power off Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
VDD12 to VDDIO timing	-	100	-	-	µs	VDD12 10% to VDDIO 10%
VDDIO to VDDMA timing	-	100	-	-	µs	VDDIO 10% to VDDMA 10%

5.4 Power State

5.4.1 State Description

Table 16. State Description

State	Description
Off	No power supply, all the voltage rails and clocks are gated.
Suspend	The sensor hardware complete power on process. The sensor enters this state when I^2C interface is ready for the host communication upon initialization complete. The sensor is available to receive command from the host. The sensor may enter this state as needed for power saving purpose while all the parameter setting still intact.
Operation	The sensor enters Operation State upon receive the host's command. This is the state where the sensor executes and deliver the required data according to host command. There is no direct interchange between Motion detection or continuous state within operation state. The sensor required to initialize when first entering to this state.
Trigger	The sensor enters this state upon receiving command for single frame capturing and output image data.

5.4.2 State Diagram

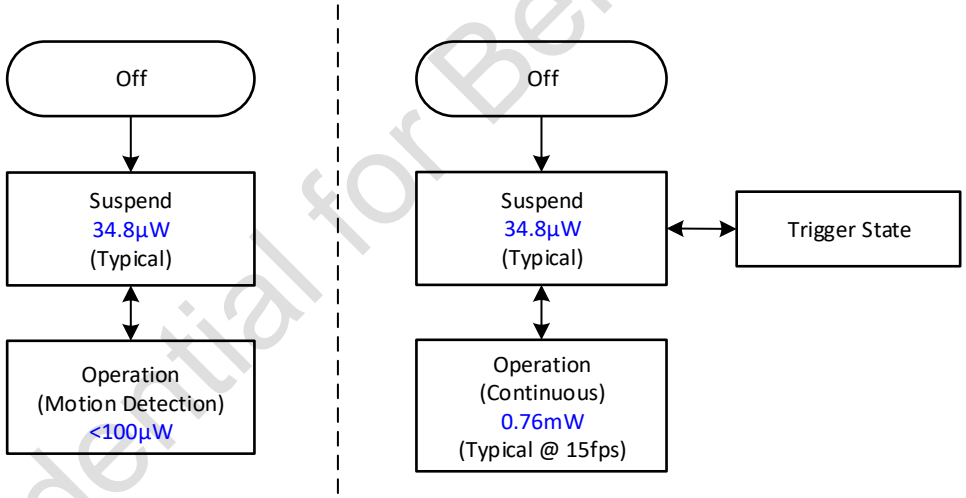


Figure 19. Power State Diagram

5.4.3 State Transition

Table 17. State Transition

State	Type	Description
Off to Suspend	Power on	Power up and transition to Ready State.
Suspend to Operation (Continuous/ Motion Detection)	Command	Enter Operation (Continuous/ Motion Detection) State by command. *R_TG_En* = 1
Operation (Continuous/ Motion detection) to Suspend	Command	Enter Suspend State by command. *R_TG_En* = 0
Operation to Trigger	Command	The host sends command to enter Trigger State. *R_TG_En* = 0 *R_Trigger_En* = 1 Using trigger event output image.
Trigger to Operation	Command	The host sends command to return Operation State. *R_Trigger_En* = 0 *R_TG_En* = 1

- Transition from Suspend to Operation (Continuous/ Motion Detection) state

Step in sequence as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x30 with value 0x01 //*R_TG_En* = 1
3. Write register 0xEB with value 0x80 //*Update flag*

- Transition from Operation (Continuous/ Motion Detection) state to Suspend

Step in sequence as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x30 with value 0x00 //*R_TG_En* = 0
3. Write register 0xEB with value 0x80 //*Update flag*

- Transition from Operation to Trigger

Step in sequence as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x30 with value 0x00 //*R_TG_En* = 0
3. Write register 0x31 with value 0x01 //*R_Trigger_En* = 1
4. Write register 0xEB with value 0x80 //*Update flag*
5. Write register 0xEA with value 0x01 //Trigger event

- Transition from Trigger to Operation

Step in sequence as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x31 with value 0x00 //*R_Trigger_En* = 0
3. Write register 0x30 with value 0x01 //*R_TG_En* = 1
4. Write register 0xEB with value 0x80 //*Update flag*

5.5 Clock

5.5.1 Description

The sensor can also work from external clock.

Table 18. External Clock Signal Description

Signal Name	Type	Ready Status	Description
GPIO1	Input	Hi-Z	Configure GPIO1 as external clock input pin.

5.5.2 Clock Specifications

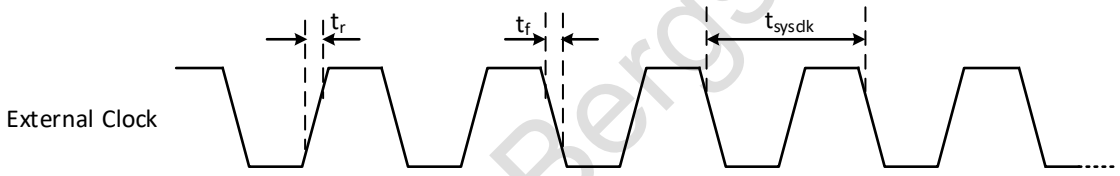


Figure 20. External Clock Timing Diagram

Table 19. External Clock Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	f_{sysclk}	-	1	-	MHz	
		-	6	-		
		-	12	-		
		-	24	-		
		-	30	-		
Period Time	t_{sysclk}	33.3	-	1000	ns	Square wave Duty cycle = 45% to 55%
Rise Time	t_R	-	-	30	ns	Voltage Level = 10% to 90% Maximum value only applies to Period Time = 1000ns
Fall Time	t_F	-	-	30	ns	Voltage Level = 90% to 10% Maximum value only applies to Period Time = 1000ns

Note: The voltage level of system clock must be the same with the level of VDDIO

5.5.3 External Clock Setting

Step in sequence as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x0E with value 0x00 //*T_GPIO1_OE* = *T_GPIO1_INL* = 0
3. Write register 0x2B with value 0x00 //*T_spll_clock* = *T_spll_refsel* = 0
4. Write register 0x36 with value 0x00 //*B_spll_EnH* = 0
5. Write register 0x29 with value 0x60 //*T_spll_postdivider* = 96
6. Write register 0x2A with value 0x10 //*T_spll_postdivider* = 96
7. Write register 0x26 with value 0x0A //Modify *T_spll_predivider*
8. Write register 0x27 with value YZ //Modify *T_spll_predivider*. YZ from Table 20.
9. Write register 0xEB with value 0x80 //*Update flag*

Table 20. *T_spll_predivider* Value for Different External Clock Frequency

External Clock Frequency (MHz)	YZ Value
1	0x41
6	0x46
12	0x4C
24	0x58
30	0x5E

5.6 Reset

The sensor supports power-on reset and software reset.

5.6.1 Power-on Reset

During power-on, the chip does not need an external reset as there is an internal circuitry that performs power-on reset function for the chip.

5.6.2 Software Reset

For software reset, write register 0xEE in bank0 with value 0xFF to trigger software reset. Typically, it is used when the chip performs mode switching between image output state (Trigger/ Continuous) and motion detection state.

5.7 Related Register

- Clock

Usage	Name	Bank	Address
External Clock Function	*T_spll_predivider[5:0]* *T_spll_predivider[8:6]*	0x00	0x27 0x26
	T_spll_postdivider[5:0] *T_spll_postdivider[8:6]*	0x00	0x29 0x2A
	T_spll_refsel *T_spll_clock*	0x00	0x2B
	B_spll_EnH	0x00	0x36

6.0 I²C Serial Interface

The sensor can configure to I²C interface. The interface is decided by the status of I²C pin.

6.1 Signal Description

The two wires used for interface communication in the sensor are SCL (clock) and SDA (data). The sensor is implemented as a slave-only device, so it never drives SCL, and only drives SDA during read cycles and transfer acknowledge bits. The sensor uses 7-bit addressing and does not support clock stretching.

Table 21. I²C Signals Description

Signal Name	Label	Type	Ready Status	Description
Serial Clock	I2C_SCL	Input	Input (Floating)	The I2C_SCL is the I²C serial clock pin and driven by the host to synchronize the serial data transmission. A pull-up resistor is required.
Serial Data	I2C_SDA	I/O	Input (Floating)	The I2C_SDA signal is data line to read from or write to the sensor. A pull-up resistor is required.

6.2 Slave ID Selection

The sensor uses 7-bit addressing and two slave ID simultaneously.

- Broadcast slave ID
- Unique slave ID; decided by the status of GPIO2 pin.

It is recommended to tie GPIO2 pin to VDDIO, floating or ground instead host control directly.

Table 22. I²C Slave ID Selection Table

Parameter	GPIO2	Note
I²C Slave Selection ID	High	I²C Slave ID: 0x25
	Floating	I²C Slave ID: 0x35
	Ground	I²C Slave ID: 0x40
I²C Slave Broadcast ID	-	I²C Slave ID: 0x60

6.3 Start and Stop of Synchronous Operation

All communications take 9 clocks to complete the 9 bits transaction, first 8 bits are for the data and the 9th bit is for acknowledge. Transfers are initiated with an S condition and terminated with the P condition. During the 8 bits of data transmissions, SDA may change while clock is low. SDA changing while clock is high is the S or P condition.

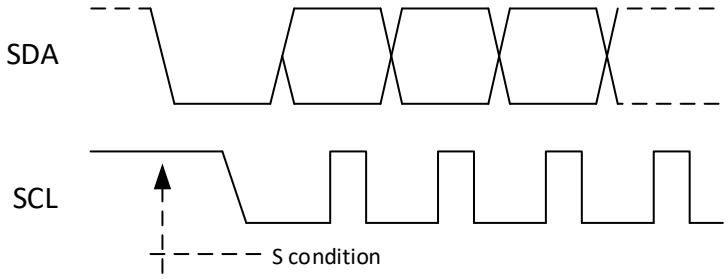


Figure 21. I²C S Conditions

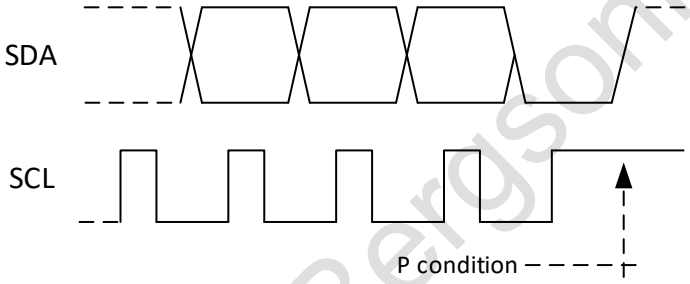


Figure 22. I²C P Conditions

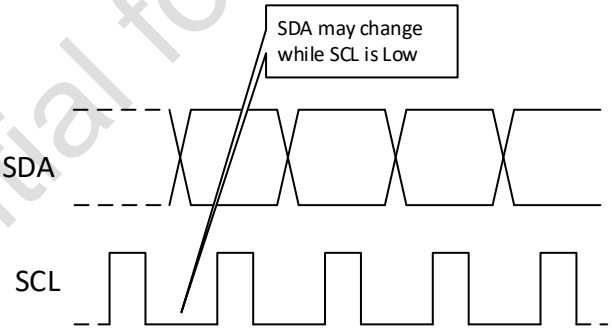


Figure 23. Data may Change when SCL is Low

Bytes that are transferred from the master to the slave are acknowledged by the slave. The slave acknowledges by driving a 0 on SDA during the 9th clock. This includes write data and slave address packets. When a byte is transferred from the slave to the master (read data), the slave ignores the SDA pin during the 9th clock.

When packets are sent over the I²C interface, they are generally of the format. The rnw (read_not_write) bit defines the direction of all data bytes after the S condition. In other words, it is not possible to initiate a write operation, and then switch to a read operation without completing the write.

S, <slave address, rnw>, A, data, A, data, A, ... , P

After a start condition, a single acknowledge/not acknowledge bit follows each eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

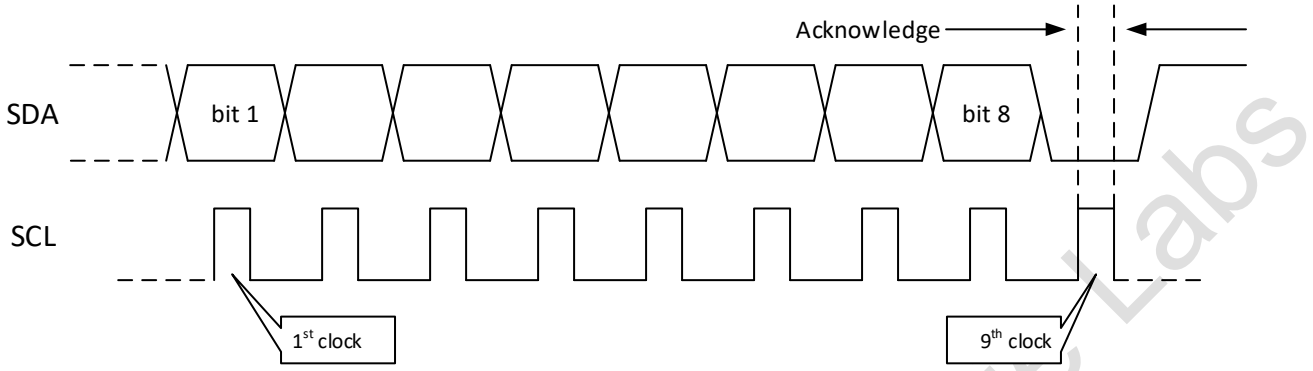


Figure 24. I²C Acknowledge Bit

6.4 Packet Format

Read and write operations between the host and the sensor use three types of host driven packets. All packets are eight bits long, with the most significant bit first, followed by an acknowledge bit.

- Slave Device Address (DA): Command packets contain a 7-bit device address and a read/write bit (R/W).
- Register Address Packets (RA): The address packets contain an 8-bit register address.
- Data Packet (DP): Contains 8 data bits, and may be sent by the host or the sensor.

Table 23. Packet Formats

Slave Device Address							
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	0: Write 1: Read
Register Address							
RA[7]	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]
Register Data							
DP[7]	DP[6]	DP[5]	DP[4]	DP[3]	DP[2]	DP[1]	DP[0]

6.5 Driven Packet

For a host driven packet, the host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the sensor then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first. To terminate the transfer of host driven packets, the host follows the sensor's ACK with a STOP condition. The host can also issue a START condition after the sensor's ACK, if it wants to start a new data transfer.

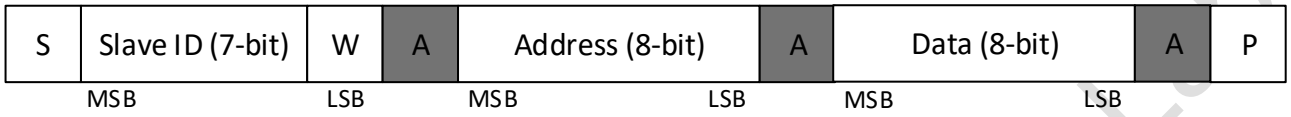


Figure 25. I²C Host Driven Packet (Write)

For a sensor driven packet, by request of the host, the sensor acknowledges a read request, and then outputs a data byte transmitting the most significant bit[7] first. If the host intends to continue the data transfer, the host acknowledges the sensor. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition, if it wants to begin a new data transfer with the same sensor.

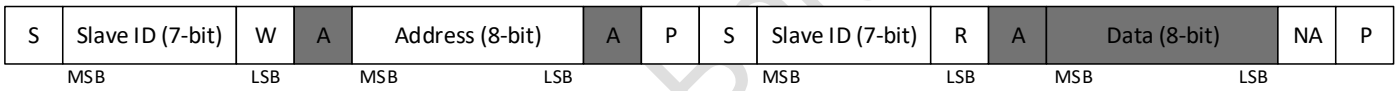


Figure 26. I²C Slave Driven Packet (Read)

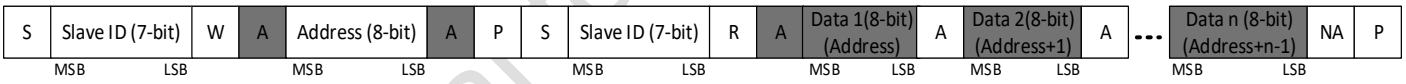


Figure 27. I²C Slave Driven Packet (Burst Read)

6.6 I²C Timing Specifications

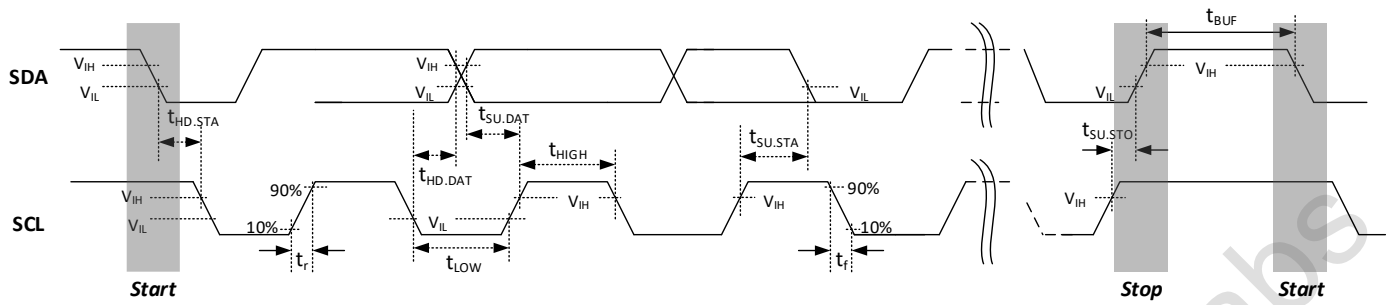


Figure 28. I²C Timing Diagram

Table 24. I²C Timing Specifications

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency.	f_{scl}	10	100	10	400	10	1000	kHz
Hold time for Start/Repeat Start. After this period, the first clock pulse is generated.	$t_{HD.STA}$	4	-	0.6	-	0.26	-	µs
Set-up time for a repeated Start.	$t_{SU.STA}$	4.7	-	0.6	-	0.26	-	µs
Low period of SCL clock.	t_{LOW}	4.7	-	1.3	-	0.5	-	µs
High period of SCL clock.	t_{HIGH}	0.75	-	0.6	-	0.26	-	µs
Data hold time.	$t_{HD.DAT}$	0	-	0	-	0	-	µs
Data set-up time.	$t_{SU.DAT}$	250	-	100	-	50	-	ns
Rise time of both SDA and SCL signals.	t_r	-	1000	-	300	-	130	ns
Fall time of both SDA and SCL signals.	t_f	-	300	-	300	-	120	ns
Set-up time for STOP condition.	$t_{SU.STO}$	4	-	0.6	-	0.26	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	1.3	-	0.5	-	µs

Note: Maximum current is 5mA and load capacitance= 100pF.

7.0 Image Output Interface

7.1 Interface Selection

The sensor has two types of image interface and can be selected through initial settings. Refer to Section 8.1.3.

- Parallel bus
- SPI bus

7.2 8-bit Parallel Communication

7.2.1 Pin Description

The parallel interface contains PXD0 to PXD7 (8-bit data), HSYNC (Horizontal Sync), VSYNC (Vertical Sync) and PXCLK (Pixel clock). All parallel signals are unidirectional and output from the sensor.

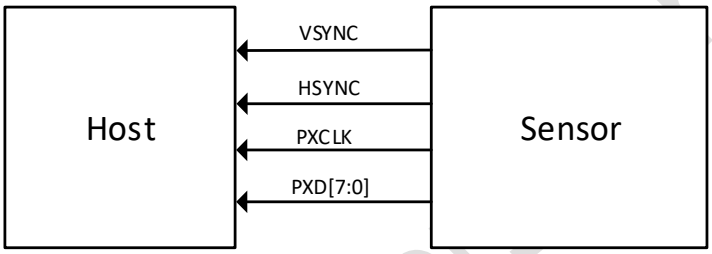


Figure 29. 8-bit Parallel Connection

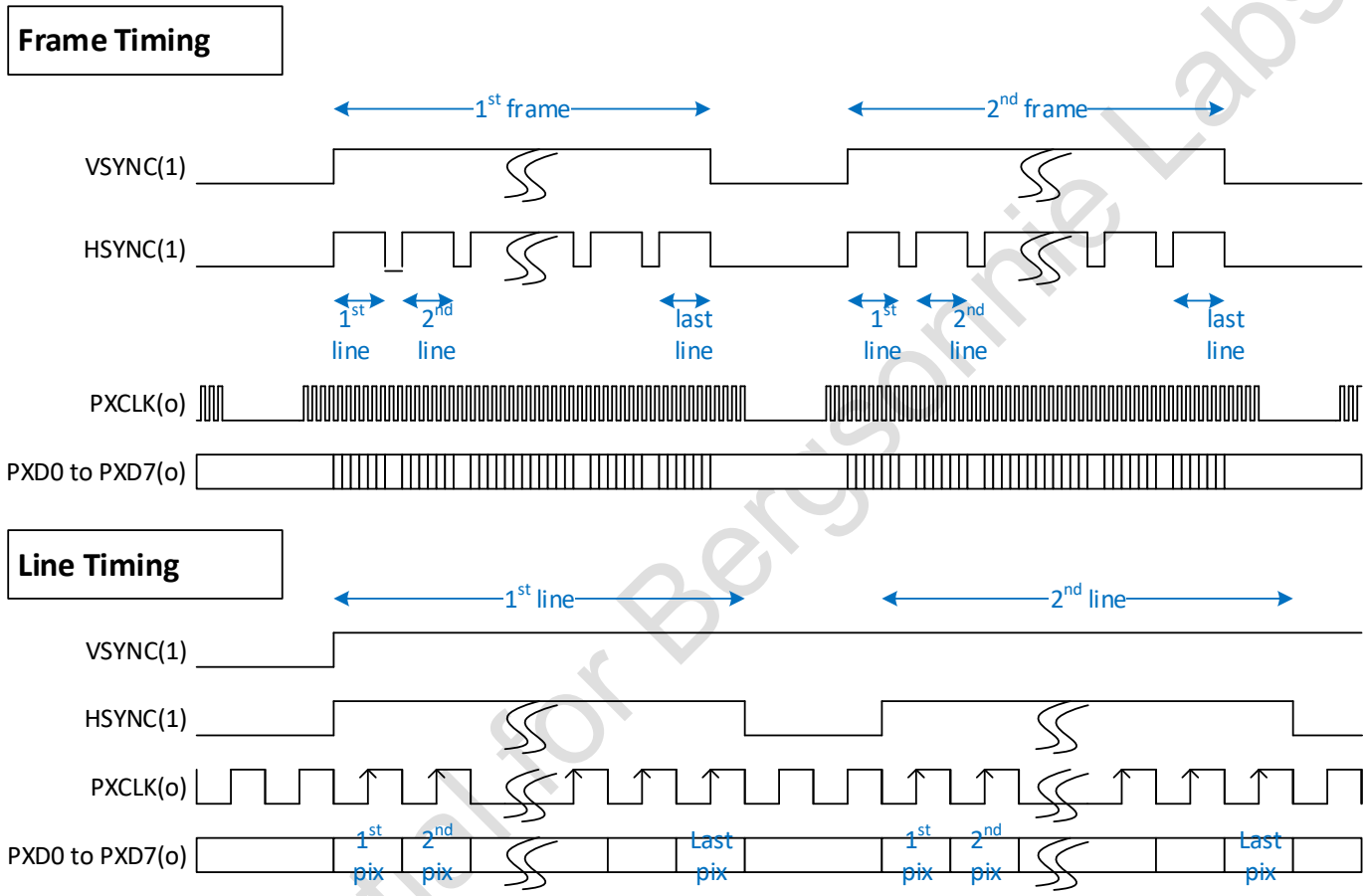
Table 25. Parallel Signal Description

Signal Name	Type	Ready Status	Description
PXD0	Output	Hi-Z	Pixel data bit[0]
PXD1	Output	Hi-Z	Pixel data bit[1]
PXD2	Output	Hi-Z	Pixel data bit[2]
PXD3	Output	Hi-Z	Pixel data bit[3]
PXD4	Output	Hi-Z	Pixel data bit[4]
PXD5	Output	Hi-Z	Pixel data bit[5]
PXD6	Output	Hi-Z	Pixel data bit[6]
PXD7	Output	Hi-Z	Pixel data bit[7]
HSYNC	Output	Hi-Z	Line signal
VSYNC	Output	Hi-Z	Frame signal
PXCLK	Output	Hi-Z	Pixel clock

7.2.2 Frame/Line Timing Sequence

By default,

- VSYNC (active high) goes high to start a frame data transfer while goes low when frame data transfer is end.
- HSYNC (active high) goes high to start a line data transfer while goes low when line data transfer is end.
- PXD0 to PXD7 output data at PXCLK falling edge while host may latch-in data at PXCLK rising edge.



Note:
The polarity of VSYNC, HSYNC and PXCLK is adjustable. The waveform above is under the setting following:
R_Parallel_Vsync_Inv=1
R_Parallel_Hsync_Inv=1
R_Parallel_Pxclk_Inv=0

Figure 30. Parallel Timing

7.2.3 Parallel Timing Specifications

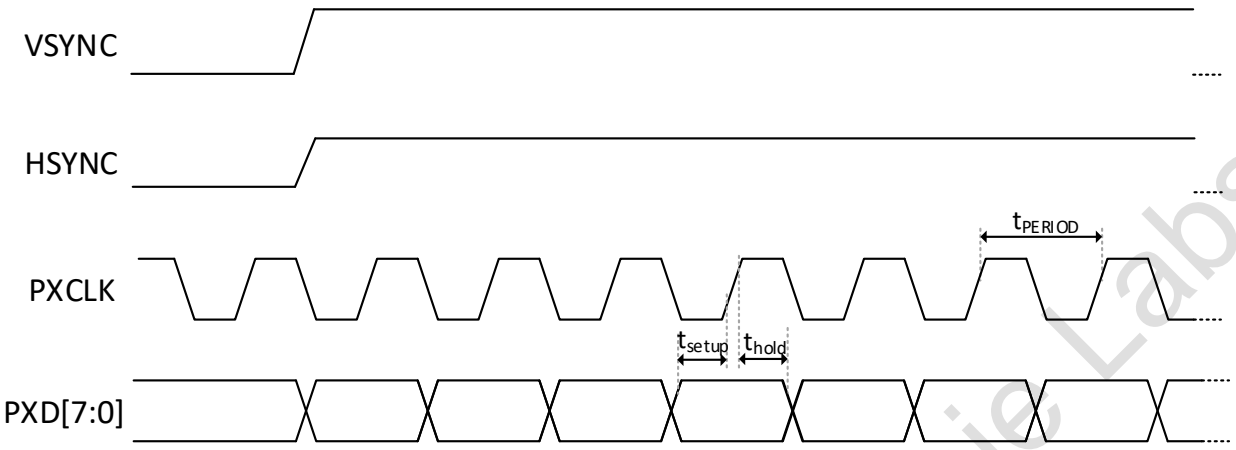


Figure 31. Parallel Timing Specifications

Table 26. Parallel Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Pixel clock frequency	f_{PXCLK}	22.8	24	25.2	MHz
PXCLK period time	t_{PEROID}	43.8	41.6	39.6	ns
Data setup time	t_{setup}	10	-	-	ns
Data hold time	t_{hold}	10	-	-	ns

Note: Clock input from external at ambient temperature= 25°C.

7.3 SPI Interface

7.3.1 Pin Description

The sensor adopts SPI mode 3 (CPHA=1 and CPOL=1) interface and configured as slave device.

The sensor supports SPI bus transfer protocol and is acting as slave device interfacing with the SPI master in the host processor.

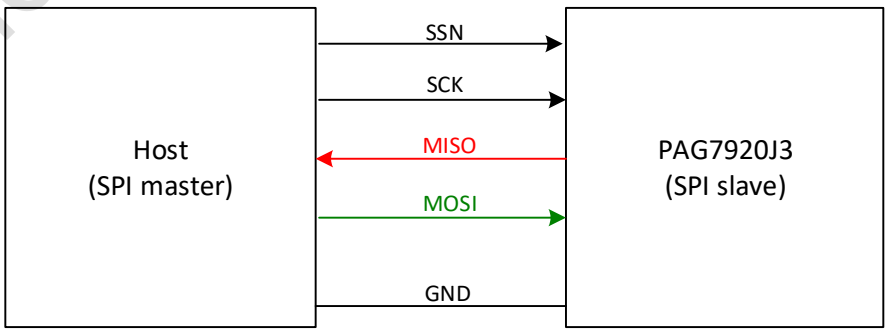


Figure 32. SPI Bus Connection

Table 27. SPI Signal Description

Signal Name	Type	Description
VSYNC/SSN	Input	SPI chip select pin
PXCLK/SCK	Input	Serial communications clock
PXD0/MISO	Output	Serial data output
HSYNC/MOSI	Input	Serial data input

7.3.2 SPI Clock Frequency

Table 28. SPI Clock Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
SPI clock frequency	-			25	MHz	

7.3.3 SPI Register Single Read/Write Operation

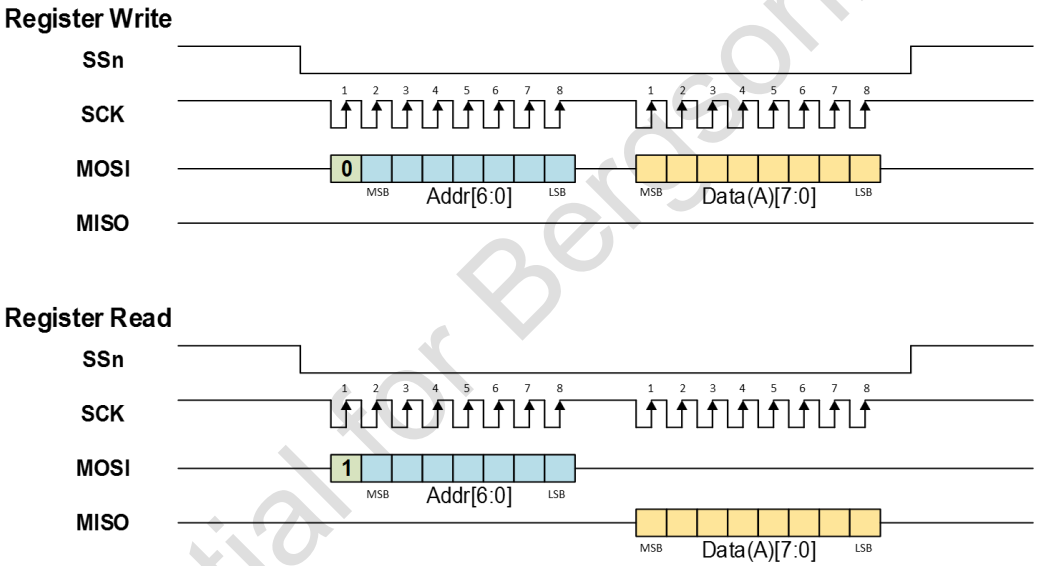


Figure 33. SPI Register Single Read/Write

7.3.4 SPI Register Burst Read/Write Operation

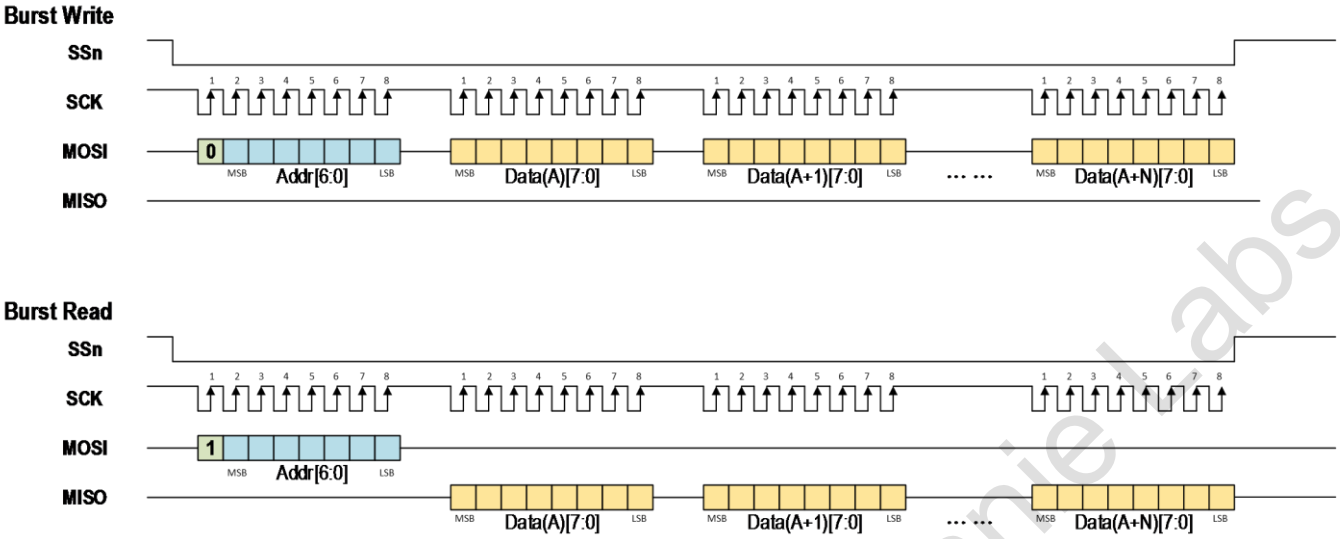


Figure 34. SPI Register Burst Read/Write

7.3.5 Related Register Accessible by SPI interface

Below is the dedicated register table that can be accessed through SPI interface.

Table 29. SPI Access Register Map

Address	Bit Field	Name	Access	Bit Field Default Value	Register Default Value
0x02	Bit[0]	R_SPI_Img_Rd_En[0]	R	-	-
0x03	-	CPU_INT0_Status[7:0]	R/W	-	0x00
0x06	-	Check ID[7:0]	R	-	-
0x07	-	Check ID[15:8]	R	-	-
0x40	-	SPI_image_data[7:0]	R	-	-

Register Name	R_SPI_Img_Rd_En[0]		
Bank	-	**Address**	0x02
Access	R	**Default Value**	-
Bit Field	**Name**	**Default Value**	**Description**
0	R_SPI_Img_Rd_En[0]	-	SPI image read enable

Register Name	CPU_INT0_Status[7:0]		
Bank	-	**Address**	0x03
Access	R/W	**Default Value**	-
Description	Interrupt status bits for SPI image mode When specific interrupt event happened, the corresponds status bit will be set to “1”. The status bits can only be cleared by host with the register command. bit[0]: FB_Rdy_INT interrupt (output buffer ready) bit[1]: Frame_Start interrupt (frame start) bit[2]: FB_Ovf_INT interrupt (output buffer overflow)		

Register Name	Check ID[7:0]		
Bank	-	**Address**	0x06
Access	R	**Default Value**	0x5A
Register Name	**Check ID[15:8]**		
Bank	-	**Address**	0x07
Access	R	**Default Value**	0xA5
Description	Check part ID. These registers can be used to examine the SPI interface is ready to use.		

Register Name	SPI_image_data[7:0]		
Bank	-	**Address**	0x40
Access	R	**Default Value**	-
Description	SPI read data		

7.3.6 Image Output Through SPI Interface

Under the SPI image output interface, the sensor outputs the image data through interrupt mechanism and the output buffer.

- Initial Configuration

1. Configure SPI image output as Image output interface through the initial setting. Refer to Section 8.1.3.
2. GPIO1 needs to configure as SPI image output interrupt signal. Refer to Section 8.6.

- Interrupt Event in SPI Interface

The SPI image output interrupt supports three interrupt events. The host needs to access *CPU_INT0_Status*[7:0] register for identification through SPI interface.

bit[0]: FB_Rdy_INT interrupt (output buffer ready)

This is an interrupt event indicates the image output buffer is ready for accessing.

bit[1]: Frame_Start interrupt (frame start)

This is an interrupt event indicates the sensor begins to transfer new frame image output to the output buffer.

bit[2]: FB_Ovf_INT interrupt (output buffer overflow)

This is an interrupt event indicates the output buffer is overflowed.

When the overflow happens, the present image output data have become invalid.

- Output Buffer Access

The following are the steps for accessing the output buffer:

1. Write register 0x02 with value 0x01 //configure *R_SPI_Img_Rd_En*=1
2. Wait for 1.5µs
3. Read register 0x40 //burst read 4800 bytes (single read is applicable too)
4. Write register 0x02 with value 0x00 //configure *R_SPI_Img_Rd_En*=0
5. Write register 0x03 with value 0xFE //configure *CPU_INT0_Status[0]*=0

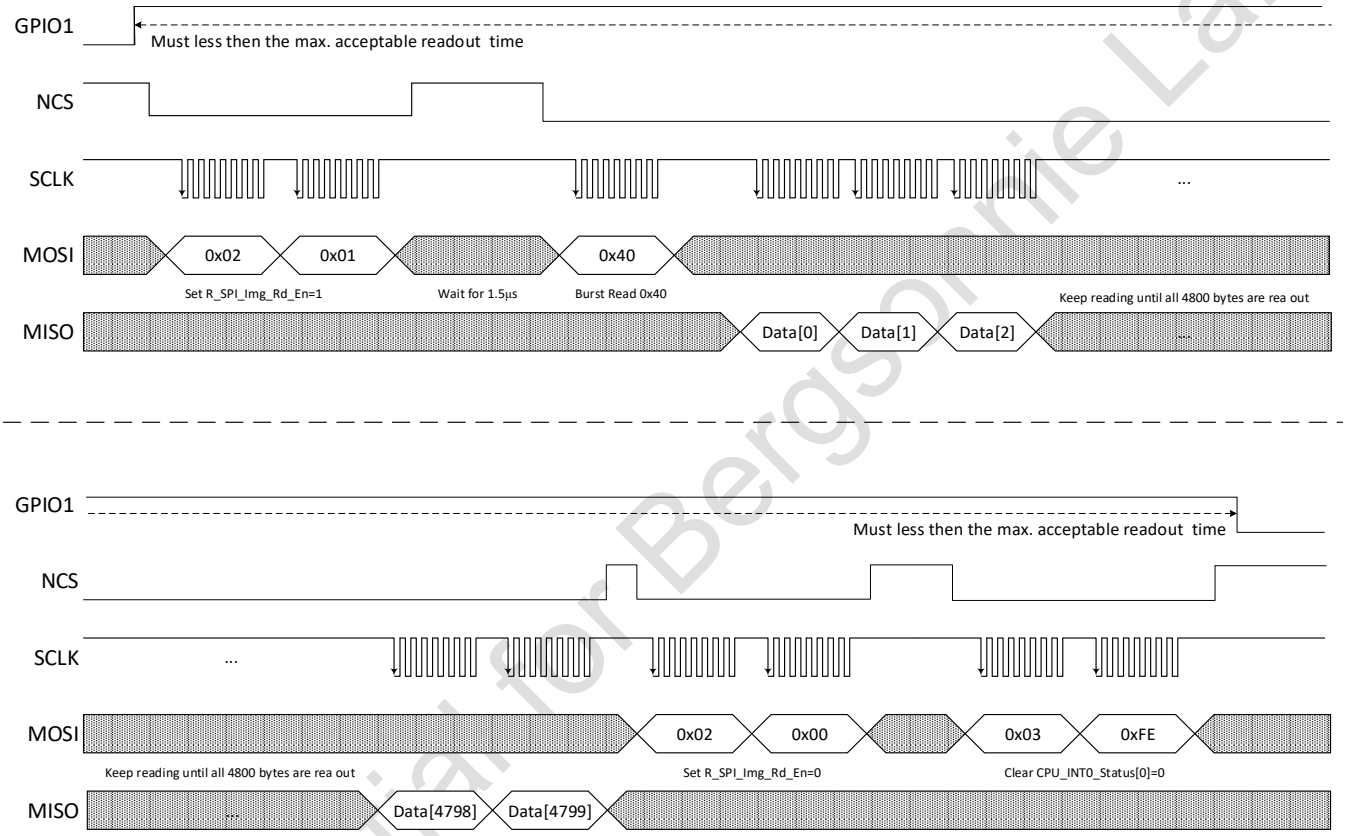


Figure 35. SPI Image Data Readout Waveform

- Output buffer and access cycle

The image frame size is depending on the image resolution.

The output buffer size is 4800 bytes. The host required to perform multiple output buffer access to complete a frame data output transmission.

Example 1:

Image size or resolution for 320 x 240 = 76800 bytes

Number of access cycle = 76800 ÷ 4800
= 16 cycles

Example 2:

Image size or resolution for 160 x 120 = 19200 bytes

Number of access cycle = 19200 ÷ 4800
= 4 cycles

- Output Buffer Access Time

The maximum output buffer access time which can be calculated by below formula

$$\text{Maximum output buffer access time, sec} = \frac{4800}{\text{H\_size}} \times \left(\text{Line Time Register Value} \times \frac{1}{\text{Half of System Clock}} \right)$$

H_size is, based on the output resolution, the pixel count of the horizontal line, e.g. 320 of QVGA

System Clock in Hz, the default System Clock is 12 MHz (SPI output).

Line Time register value can be read from *R_LineTime* registers.

For example,

SPI output with QVGA and default system clock 12 MHz, the maximum output buffer access time is around 3.39ms.

- Reference control flow for SPI interrupt handling

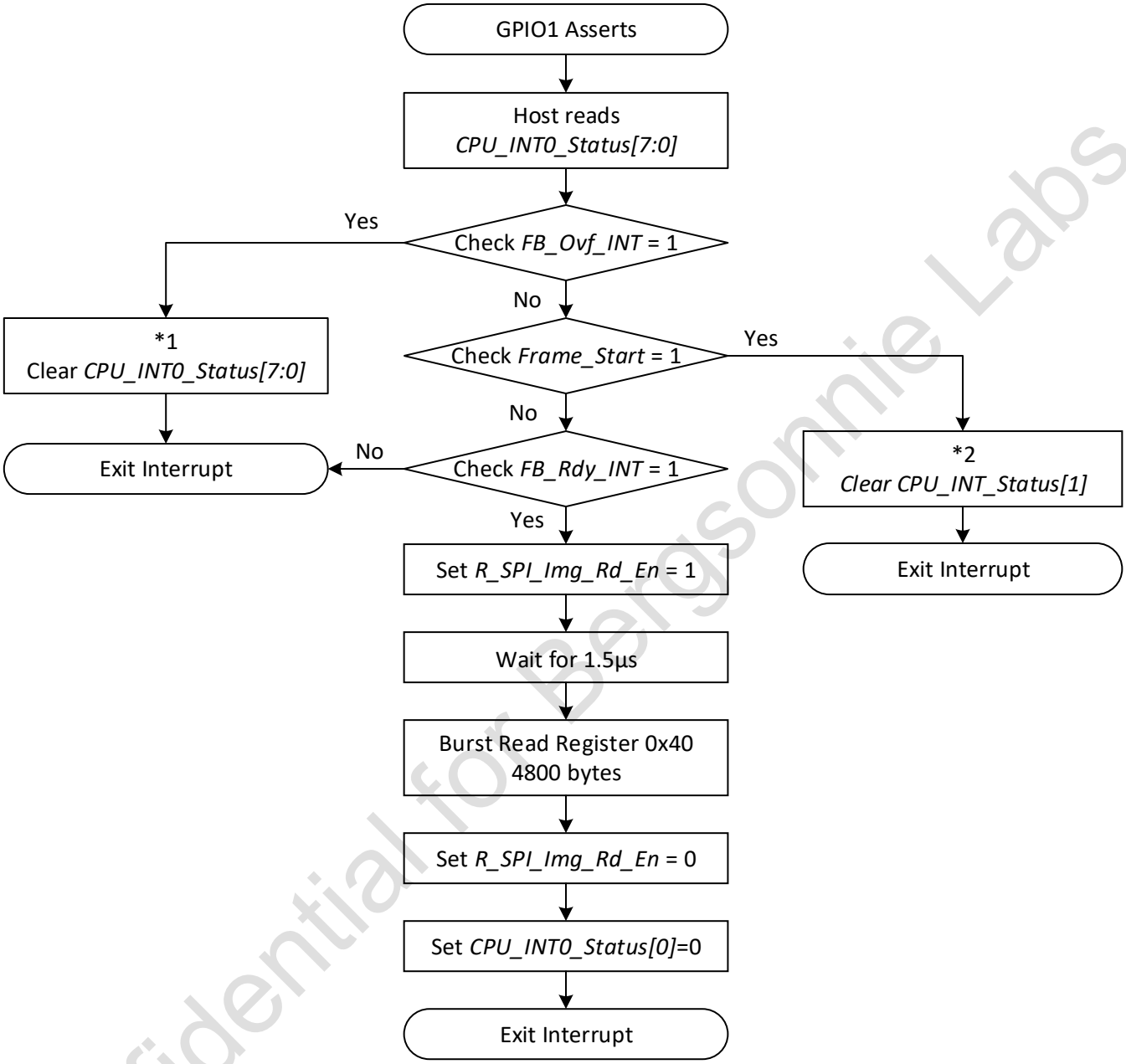


Figure 36. Reference SPI Interrupt Handling Flow

Notes:

*1: The overflow interrupt has happened; the present image output data have become invalid.

*2: Begin transfer new frame image output.

7.4 Related Register

Usage	Name	Bank	Address
Set parallel interface clock	Parallel Interface Polarity	0x00	0xAF
Line Time Adjustment	*R_LineTime[7:0]* *R_LineTime[13:8]*	0x02	0xC1 0xC2

8.0 System Control

8.1 System Initialization

The successful of Part ID read is to confirm the I²C interface is working as normal.

8.1.1 Power-on Setup Time

The sensor supports bootstrapping function. During initialization stage, GPIO2 pin is configured to one out of three I²C slave ID address. (Refer to Table 22)

The I²C slave ID is captured 30ms after power-on as shown in Figure 37.

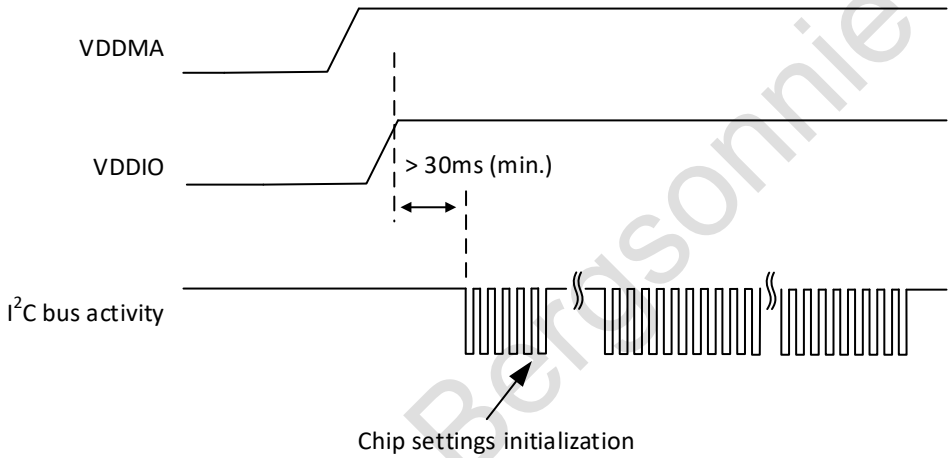


Figure 37. Power-on Sequence Requirement

8.1.2 Initialization Flow

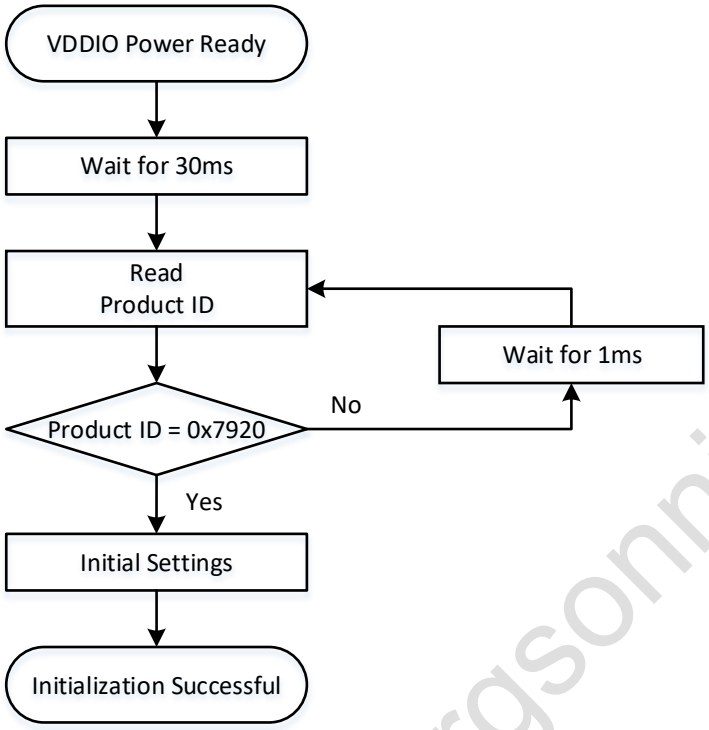


Figure 38. System Initialization Flow Chart

Note:

1. If the sensor ID read not successful, it is recommended to power off and power on the sensor again. If the problem persists, do check the I^2C interface connection and settings.
2. Upon successful of initialization, refer to Section 4.2 for entering the targeted operation state.

8.1.3 Initialization Setting

Upon the sensor power up completion, the host need to configure the registers setting. The selection of initial settings below is based on application requirement. For change of state and resolution, it must be reset from power off to power on.

No	Interface	Mode	Resolution	Analog Skip	Analog Average	Initial Setting Configuration
1	Parallel	Continuous Image Out /Trigger	320 x 240	1x	1x	Section 8.1.3.1
2			160 x 120	2x	1x	Section 8.1.3.1+Section 8.1.3.2
3			160 x 120	1x	2x	Section 8.1.3.1+Section 8.1.3.3
4	SPI	Continuous Image Out /Trigger	320 x 240	1x	1x	Section 8.1.3.4+Section 8.1.3.5
5			160 x 120	2x	1x	Section 8.1.3.4+Section 8.1.3.6
6			160 x 120	1x	2x	Section 8.1.3.4+Section 8.1.3.7
7	-	Motion Detection	80x60	-	-	Section 8.1.3.8

8.1.3.1 320x240 (Default QVGA resolution), Parallel Out

1. Write register 0xEF with value 0x00
2. Write register 0x1D with value 0x41
3. Write register 0x64 with value 0x01
4. Write register 0x45 with value 0x44
5. Write register 0x12 with value 0x20
6. Write register 0x0C with value 0xC8
7. Write register 0x11 with value 0xC8
8. Write register 0x42 with value 0xC8
9. Write register 0x43 with value 0xC8
10. Write register 0x44 with value 0xC8
11. Write register 0xAF with value 0x31
12. Write register 0x69 with value 0x14
13. Write register 0xEF with value 0x00
14. Write register 0x23 with value 0x87
15. Write register 0x26 with value 0x1A
16. Write register 0x27 with value 0x60
17. Write register 0x29 with value 0x00
18. Write register 0x2A with value 0x30
19. Write register 0x2B with value 0x02
20. Write register 0x36 with value 0x00
21. Write register 0xEF with value 0x00
22. Write register 0x4C with value 0x00
23. Write register 0x4D with value 0x35
24. Write register 0x4E with value 0x0C
25. Write register 0x4F with value 0x00
26. Write register 0xEF with value 0x02
27. Write register 0x02 with value 0x64
28. Write register 0x03 with value 0x08
29. Write register 0x29 with value 0x64
30. Write register 0x2A with value 0x00
31. Write register 0x2B with value 0x64
32. Write register 0x2C with value 0x00
33. Write register 0x31 with value 0x64
34. Write register 0x32 with value 0x00
35. Write register 0x46 with value 0x00
36. Write register 0x47 with value 0x46
37. Write register 0x48 with value 0x00
38. Write register 0x49 with value 0x01
39. Write register 0x4A with value 0x00
40. Write register 0x4B with value 0x00
41. Write register 0x5B with value 0x01
42. Write register 0xEF with value 0x04
43. Write register 0x2C with value 0xC6
44. Write register 0x2D with value 0x2D
45. Write register 0x2E with value 0x00
46. Write register 0x30 with value 0x31
47. Write register 0x31 with value 0x80
48. Write register 0x40 with value 0x1D
49. Write register 0x41 with value 0x00
50. Write register 0x42 with value 0xD0
51. Write register 0x43 with value 0x01
52. Write register 0x44 with value 0xF0
53. Write register 0x45 with value 0x00
54. Write register 0x46 with value 0x00
55. Write register 0x47 with value 0x00
56. Write register 0x48 with value 0xF0
57. Write register 0x49 with value 0x0D
58. Write register 0x4A with value 0x0C
59. Write register 0x4B with value 0x00
60. Write register 0x50 with value 0x22
61. Write register 0x51 with value 0x1D
62. Write register 0x52 with value 0x00
63. Write register 0x53 with value 0xC0
64. Write register 0x54 with value 0xD4
65. Write register 0x55 with value 0x01
66. Write register 0x56 with value 0x00
67. Write register 0xEF with value 0x01
68. Write register 0xC4 with value 0x02
69. Write register 0xC6 with value 0x40
70. Write register 0xC7 with value 0x01
71. Write register 0xC8 with value 0xF0
72. Write register 0xC9 with value 0x00
73. Write register 0xEF with value 0x02
74. Write register 0x11 with value 0x03
75. Write register 0x19 with value 0xFC
76. Write register 0x1A with value 0x00
77. Write register 0x21 with value 0x40
78. Write register 0x22 with value 0x01
79. Write register 0x23 with value 0xF0
80. Write register 0x24 with value 0x00

81. Write register 0x27 with value 0x0C
82. Write register 0x28 with value 0x00
83. Write register 0x2D with value 0xF0
84. Write register 0x2E with value 0x00
85. Write register 0x56 with value 0x40
86. Write register 0x57 with value 0x01
87. Write register 0x58 with value 0xFE
88. Write register 0x59 with value 0x00
89. Write register 0xEF with value 0x01
90. Write register 0x33 with value 0x46
91. Write register 0x3B with value 0x30
92. Write register 0x40 with value 0x96
93. Write register 0xD9 with value 0x32
94. Write register 0xDB with value 0x64
95. Write register 0xDD with value 0x64
96. Write register 0xEF with value 0x02
97. Write register 0xA5 with value 0x00
98. Write register 0xA6 with value 0x96
99. Write register 0xEF with value 0x00
100. Write register 0x09 with value 0x10
101. Write register 0x18 with value 0x01
102. Write register 0x2F with value 0x44
103. Write register 0x37 with value 0x04
104. Write register 0x38 with value 0x06
105. Write register 0x3F with value 0x01
106. Write register 0x55 with value 0x01
107. Write register 0x66 with value 0x01
108. Write register 0xEF with value 0x01
109. Write register 0x03 with value 0x00
110. Write register 0x04 with value 0xAB
111. Write register 0x07 with value 0x02
112. Write register 0x0A with value 0x00
113. Write register 0x0B with value 0x40
114. Write register 0x0F with value 0x0B
115. Write register 0x11 with value 0x0A
116. Write register 0x13 with value 0x0C
117. Write register 0x16 with value 0x00
118. Write register 0x17 with value 0xA9
119. Write register 0x36 with value 0x00
120. Write register 0x37 with value 0x02
121. Write register 0x4D with value 0x02
122. Write register 0x56 with value 0xB8
123. Write register 0x57 with value 0x01
124. Write register 0x58 with value 0xB8
125. Write register 0x59 with value 0x01
126. Write register 0x62 with value 0x00
127. Write register 0x63 with value 0x06
128. Write register 0x69 with value 0x1C
129. Write register 0x6A with value 0x1D
130. Write register 0x6B with value 0x68
131. Write register 0x6C with value 0x67
132. Write register 0x76 with value 0x06
133. Write register 0x77 with value 0x09
134. Write register 0x78 with value 0x02
135. Write register 0x79 with value 0x03
136. Write register 0x84 with value 0x19
137. Write register 0x86 with value 0x14
138. Write register 0x87 with value 0x19
139. Write register 0x89 with value 0x14
140. Write register 0x8A with value 0x23
141. Write register 0x8C with value 0x1E
142. Write register 0x8D with value 0x23
143. Write register 0x8F with value 0x1E
144. Write register 0x9D with value 0x0A
145. Write register 0xA0 with value 0x00
146. Write register 0xD1 with value 0xC8
147. Write register 0xD2 with value 0x00
148. Write register 0xEF with value 0x02
149. Write register 0x92 with value 0x11
150. Write register 0x93 with value 0x01
151. Write register 0xC3 with value 0xC8
152. Write register 0xC4 with value 0x00
153. Write register 0xC5 with value 0xC8
154. Write register 0xC6 with value 0x00
155. Write register 0xD1 with value 0x45
156. Write register 0xEF with value 0x00
157. Write register 0xEB with value 0x80
158. Write register 0xEF with value 0x00
159. Write register 0x30 with value 0x01

8.1.3.2 160x120, Analog 2x Skip, Parallel Out

Set "Section 8.1.3.1" setting first, then apply "Section 8.1.3.2" setting as below.

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x00
3. Write register 0x15 with value 0x0C
4. Write register 0x16 with value 0x6D
5. Write register 0x1C with value 0x00
6. Write register 0x3E with value 0x20
7. Write register 0xEF with value 0x01
8. Write register 0x4B with value 0x11
9. Write register 0x70 with value 0x10
10. Write register 0xC2 with value 0x02
11. Write register 0xC3 with value 0x00
12. Write register 0xC8 with value 0x78
13. Write register 0xC9 with value 0x00
14. Write register 0xCB with value 0x04
15. Write register 0xCC with value 0x00
16. Write register 0xCE with value 0x00
17. Write register 0xEF with value 0x02
18. Write register 0x19 with value 0x81
19. Write register 0x1A with value 0x00
20. Write register 0x23 with value 0x78
21. Write register 0x24 with value 0x00
22. Write register 0x27 with value 0x09
23. Write register 0x28 with value 0x00
24. Write register 0x2D with value 0x78
25. Write register 0x2E with value 0x00
26. Write register 0xD9 with value 0x01
27. Write register 0xEF with value 0x04
28. Write register 0x3A with value 0x28
29. Write register 0x3B with value 0x1E
30. Write register 0xEF with value 0x00
31. Write register 0xEB with value 0x80
32. Write register 0x30 with value 0x01

8.1.3.3 160x120, Analog 2x Average, Parallel Out

Set "Section 8.1.3.1" setting first, then apply "Section 8.1.3.3" setting as below.

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x00
3. Write register 0x15 with value 0x2C
4. Write register 0x16 with value 0x6D
5. Write register 0x1C with value 0x02
6. Write register 0x3E with value 0x04
7. Write register 0xEF with value 0x01
8. Write register 0x4B with value 0x11
9. Write register 0x70 with value 0x10
10. Write register 0xC2 with value 0x02
11. Write register 0xC3 with value 0x00
12. Write register 0xC8 with value 0x78
13. Write register 0xC9 with value 0x00
14. Write register 0xCB with value 0x04
15. Write register 0xCC with value 0x00
16. Write register 0xCE with value 0x00
17. Write register 0xEF with value 0x02
18. Write register 0x19 with value 0x81
19. Write register 0x1A with value 0x00
20. Write register 0x23 with value 0x78
21. Write register 0x24 with value 0x00
22. Write register 0x27 with value 0x09
23. Write register 0x28 with value 0x00
24. Write register 0x2D with value 0x78
25. Write register 0x2E with value 0x00
26. Write register 0xD9 with value 0x01
27. Write register 0xEF with value 0x04
28. Write register 0x3A with value 0x28
29. Write register 0x3B with value 0x1E
30. Write register 0xEF with value 0x00
31. Write register 0xEB with value 0x80
32. Write register 0x30 with value 0x01

8.1.3.4 Default, SPI Out

1. Write register 0xEF with value 0x00
2. Write register 0x1D with value 0x81
3. Write register 0x64 with value 0x02
4. Write register 0x45 with value 0x44
5. Write register 0x12 with value 0x20
6. Write register 0x0C with value 0xC8
7. Write register 0x11 with value 0xC8
8. Write register 0x42 with value 0xC8
9. Write register 0x43 with value 0xC8
10. Write register 0x44 with value 0xC8
11. Write register 0xAF with value 0x31
12. Write register 0x69 with value 0x14
13. Write register 0x23 with value 0x87
14. Write register 0x26 with value 0x1A
15. Write register 0x27 with value 0x60
16. Write register 0x29 with value 0x00
17. Write register 0x2A with value 0x30
18. Write register 0x2B with value 0x02
19. Write register 0x36 with value 0x00
20. Write register 0x4C with value 0x80
21. Write register 0x4D with value 0x1A
22. Write register 0x4E with value 0x06
23. Write register 0x4F with value 0x00
24. Write register 0xEF with value 0x02
25. Write register 0x02 with value 0x64
26. Write register 0x03 with value 0x08
27. Write register 0x29 with value 0x64
28. Write register 0x2A with value 0x00
29. Write register 0x2B with value 0x64
30. Write register 0x2C with value 0x00
31. Write register 0x31 with value 0x64
32. Write register 0x32 with value 0x00
33. Write register 0x46 with value 0x00
34. Write register 0x47 with value 0x46
35. Write register 0x48 with value 0x00
36. Write register 0x49 with value 0x01
37. Write register 0x4A with value 0x00
38. Write register 0x4B with value 0x00
39. Write register 0x5B with value 0x01
40. Write register 0xEF with value 0x04
41. Write register 0x2C with value 0xE3
42. Write register 0x2D with value 0x16
43. Write register 0x2E with value 0x00
44. Write register 0x30 with value 0x31
45. Write register 0x31 with value 0x80
46. Write register 0x40 with value 0x1D
47. Write register 0x41 with value 0x00
48. Write register 0x42 with value 0xA0
49. Write register 0x43 with value 0x03
50. Write register 0x44 with value 0xF0
51. Write register 0x45 with value 0x00
52. Write register 0x46 with value 0x00
53. Write register 0x47 with value 0x00
54. Write register 0x48 with value 0x70
55. Write register 0x49 with value 0xF3
56. Write register 0x4A with value 0x05
57. Write register 0x4B with value 0x00
58. Write register 0x50 with value 0x22
59. Write register 0x51 with value 0x1D
60. Write register 0x52 with value 0x00
61. Write register 0x53 with value 0xC0
62. Write register 0x54 with value 0xD4
63. Write register 0x55 with value 0x01
64. Write register 0x56 with value 0x00
65. Write register 0xEF with value 0x01
66. Write register 0xC4 with value 0x02
67. Write register 0xC6 with value 0x40
68. Write register 0xC7 with value 0x01
69. Write register 0xC8 with value 0xF0
70. Write register 0xC9 with value 0x00
71. Write register 0xEF with value 0x02
72. Write register 0x11 with value 0x03
73. Write register 0x19 with value 0xFC
74. Write register 0x1A with value 0x00
75. Write register 0x21 with value 0x40
76. Write register 0x22 with value 0x01
77. Write register 0x23 with value 0xF0
78. Write register 0x24 with value 0x00
79. Write register 0x27 with value 0x0C
80. Write register 0x28 with value 0x00

81. Write register 0x2D with value 0xF0
82. Write register 0x2E with value 0x00
83. Write register 0x56 with value 0x40
84. Write register 0x57 with value 0x01
85. Write register 0x58 with value 0xFE
86. Write register 0x59 with value 0x00
87. Write register 0xEF with value 0x01
88. Write register 0x33 with value 0x23
89. Write register 0x3B with value 0x18
90. Write register 0x40 with value 0x50
91. Write register 0xD9 with value 0x19
92. Write register 0xDB with value 0x32
93. Write register 0xDD with value 0x32
94. Write register 0xEF with value 0x02
95. Write register 0xA5 with value 0x00
96. Write register 0xA6 with value 0x50
97. Write register 0xEF with value 0x00
98. Write register 0x09 with value 0x10
99. Write register 0x18 with value 0x01
100. Write register 0x2F with value 0x44
101. Write register 0x37 with value 0x04
102. Write register 0x38 with value 0x06
103. Write register 0x3F with value 0x01
104. Write register 0x55 with value 0x01
105. Write register 0x66 with value 0x01
106. Write register 0xEF with value 0x01
107. Write register 0x03 with value 0x00
108. Write register 0x04 with value 0xAB
109. Write register 0x07 with value 0x02
110. Write register 0x0A with value 0x00
111. Write register 0x0B with value 0x4C
112. Write register 0x0F with value 0x15
113. Write register 0x11 with value 0x14
114. Write register 0x13 with value 0x16
115. Write register 0x16 with value 0x00
116. Write register 0x17 with value 0xA9
117. Write register 0x36 with value 0x00
118. Write register 0x37 with value 0x02
119. Write register 0x4D with value 0x02
120. Write register 0x56 with value 0xB8
121. Write register 0x57 with value 0x01
122. Write register 0x58 with value 0xB8
123. Write register 0x59 with value 0x01
124. Write register 0x62 with value 0x00
125. Write register 0x63 with value 0x06
126. Write register 0x69 with value 0x0F
127. Write register 0x6A with value 0x0F
128. Write register 0x6B with value 0x37
129. Write register 0x6C with value 0x37
130. Write register 0x76 with value 0x06
131. Write register 0x77 with value 0x09
132. Write register 0x78 with value 0x02
133. Write register 0x79 with value 0x03
134. Write register 0x84 with value 0x23
135. Write register 0x86 with value 0x1E
136. Write register 0x87 with value 0x23
137. Write register 0x89 with value 0x1E
138. Write register 0x8A with value 0x3C
139. Write register 0x8C with value 0x32
140. Write register 0x8D with value 0x3C
141. Write register 0x8F with value 0x32
142. Write register 0x9D with value 0x14
143. Write register 0xA0 with value 0x00
144. Write register 0xD1 with value 0xB9
145. Write register 0xD2 with value 0x00
146. Write register 0xEF with value 0x02
147. Write register 0x92 with value 0x11
148. Write register 0x93 with value 0x01
149. Write register 0xC3 with value 0xB9
150. Write register 0xC4 with value 0x00
151. Write register 0xC5 with value 0xB9
152. Write register 0xC6 with value 0x00
153. Write register 0xD1 with value 0x45
154. Write register 0xEF with value 0x00
155. Write register 0xEB with value 0x80
156. Write register 0x30 with value 0x01

8.1.3.5 320x240 (Default QVGA resolution), SPI Out

Set "Section 8.1.3.4" setting first, then apply "Section 8.1.3.5" setting as below.

1. Write register 0xEF with value 0x00
2. Write register 0xE5 with value 0x07
3. Write register 0xE5 with value 0x03
4. Write register 0xE5 with value 0x01
5. Write register 0xE5 with value 0x00
6. Write register 0x1D with value 0x81
7. Write register 0x64 with value 0x02
8. Write register 0x0C with value 0xC8
9. Write register 0x11 with value 0xC8
10. Write register 0x42 with value 0x08
11. Write register 0x43 with value 0x08
12. Write register 0x44 with value 0x08
13. Write register 0x0E with value 0xC0
14. Write register 0x07 with value 0x04
15. Write register 0x32 with value 0x32
16. Write register 0xEF with value 0x02
17. Write register 0xC1 with value 0x4D
18. Write register 0xC2 with value 0x05
19. Write register 0xC7 with value 0x01
20. Write register 0xEF with value 0x00
21. Write register 0x30 with value 0x01
22. Write register 0xEF with value 0x00
23. Write register 0xB0 with value 0x01

8.1.3.6 160x120, Analog 2x Skip, SPI Out

Set "Section 8.1.3.4" setting first, then apply "Section 8.1.3.6" setting as below.

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x00
3. Write register 0x15 with value 0x0C
4. Write register 0x16 with value 0x6D
5. Write register 0x1C with value 0x00
6. Write register 0x3E with value 0x20
7. Write register 0xEF with value 0x01
8. Write register 0x4B with value 0x11
9. Write register 0x70 with value 0x10
10. Write register 0xC2 with value 0x02
11. Write register 0xC3 with value 0x00
12. Write register 0xC8 with value 0x78
13. Write register 0xC9 with value 0x00
14. Write register 0xCB with value 0x04
15. Write register 0xCC with value 0x00
16. Write register 0xCE with value 0x00
17. Write register 0xEF with value 0x02
18. Write register 0x19 with value 0x81
19. Write register 0x1A with value 0x00
20. Write register 0x23 with value 0x78
21. Write register 0x24 with value 0x00
22. Write register 0x27 with value 0x09
23. Write register 0x28 with value 0x00
24. Write register 0x2D with value 0x78
25. Write register 0x2E with value 0x00
26. Write register 0xD9 with value 0x01
27. Write register 0xEF with value 0x04
28. Write register 0x3A with value 0x28
29. Write register 0x3B with value 0x1E
30. Write register 0xEF with value 0x00
31. Write register 0xEB with value 0x80
32. Write register 0x30 with value 0x01
33. Write register 0xE5 with value 0x07
34. Write register 0xE5 with value 0x03
35. Write register 0xE5 with value 0x01
36. Write register 0xE5 with value 0x00
37. Write register 0x1D with value 0x81
38. Write register 0x64 with value 0x02
39. Write register 0x0C with value 0xC8
40. Write register 0x11 with value 0xC8
41. Write register 0x42 with value 0x08
42. Write register 0x43 with value 0x08
43. Write register 0x44 with value 0x08
44. Write register 0x0E with value 0xC0
45. Write register 0x07 with value 0x04
46. Write register 0x32 with value 0x32

47. Write register 0xEF with value 0x02
48. Write register 0xC1 with value 0x4D
49. Write register 0xC2 with value 0x05
50. Write register 0xC7 with value 0x01
51. Write register 0xEF with value 0x00
52. Write register 0x7A with value 0x10
53. Write register 0x30 with value 0x01
54. Write register 0xEF with value 0x00
55. Write register 0xB0 with value 0x01

8.1.3.7 160x120, Analog 2x Average, SPI Out

Set "Section 8.1.3.4" setting first, then apply "Section 8.1.3.7" setting as below.

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x00
3. Write register 0x15 with value 0x2C
4. Write register 0x16 with value 0x6D
5. Write register 0x1C with value 0x02
6. Write register 0x3E with value 0x04
7. Write register 0xEF with value 0x01
8. Write register 0x4B with value 0x11
9. Write register 0x70 with value 0x10
10. Write register 0xC2 with value 0x02
11. Write register 0xC3 with value 0x00
12. Write register 0xC8 with value 0x78
13. Write register 0xC9 with value 0x00
14. Write register 0xCB with value 0x04
15. Write register 0xCC with value 0x00
16. Write register 0xCE with value 0x00
17. Write register 0xEF with value 0x02
18. Write register 0x19 with value 0x81
19. Write register 0x1A with value 0x00
20. Write register 0x23 with value 0x78
21. Write register 0x24 with value 0x00
22. Write register 0x27 with value 0x09
23. Write register 0x28 with value 0x00
24. Write register 0x2D with value 0x78
25. Write register 0x2E with value 0x00
26. Write register 0xD9 with value 0x01
27. Write register 0xEF with value 0x04
28. Write register 0x3A with value 0x28
29. Write register 0x3B with value 0x1E
30. Write register 0xEF with value 0x00
31. Write register 0xEB with value 0x80
32. Write register 0x30 with value 0x01
33. Write register 0xE5 with value 0x07
34. Write register 0xE5 with value 0x03
35. Write register 0xE5 with value 0x01
36. Write register 0xE5 with value 0x00
37. Write register 0x1D with value 0x81
38. Write register 0x64 with value 0x02
39. Write register 0x0C with value 0xC8
40. Write register 0x11 with value 0xC8
41. Write register 0x42 with value 0x08
42. Write register 0x43 with value 0x08
43. Write register 0x44 with value 0x08
44. Write register 0x0E with value 0xC0
45. Write register 0x07 with value 0x04
46. Write register 0x32 with value 0x32
47. Write register 0xEF with value 0x02
48. Write register 0xC1 with value 0x4D
49. Write register 0xC2 with value 0x05
50. Write register 0xC7 with value 0x01
51. Write register 0xEF with value 0x00
52. Write register 0x7A with value 0x10
53. Write register 0x30 with value 0x01
54. Write register 0xEF with value 0x00
55. Write register 0xB0 with value 0x01

8.1.3.8 Default, Motion

1. Write register 0xEF with value 0x00
2. Write register 0x45 with value 0x44
3. Write register 0x12 with value 0x20
4. Write register 0x0C with value 0xC8
5. Write register 0x11 with value 0xC8
6. Write register 0x42 with value 0xC8
7. Write register 0x43 with value 0xC8
8. Write register 0x44 with value 0xC8
9. Write register 0xAF with value 0x33
10. Write register 0x4C with value 0x80
11. Write register 0x4D with value 0x8D
12. Write register 0x4E with value 0x5B
13. Write register 0x4F with value 0x00
14. Write register 0x23 with value 0x87
15. Write register 0x26 with value 0x1A
16. Write register 0x27 with value 0x60
17. Write register 0x29 with value 0x00
18. Write register 0x2A with value 0x30
19. Write register 0x2B with value 0x02
20. Write register 0x36 with value 0x00
21. Write register 0xEF with value 0x04
22. Write register 0x30 with value 0x31
23. Write register 0x31 with value 0x80
24. Write register 0x38 with value 0x00
25. Write register 0x39 with value 0x00
26. Write register 0x3A with value 0x14
27. Write register 0x3B with value 0x0F
28. Write register 0x40 with value 0x1D
29. Write register 0x41 with value 0x00
30. Write register 0x42 with value 0xA0
31. Write register 0x43 with value 0x03
32. Write register 0x44 with value 0xF0
33. Write register 0x45 with value 0x00
34. Write register 0x46 with value 0x00
35. Write register 0x47 with value 0x00
36. Write register 0x48 with value 0x70
37. Write register 0x49 with value 0x66
38. Write register 0x4A with value 0x5B
39. Write register 0x4B with value 0x00
40. Write register 0xEF with value 0x01
41. Write register 0xC6 with value 0x50
42. Write register 0xC7 with value 0x00
43. Write register 0xC8 with value 0x3C
44. Write register 0xC9 with value 0x00
45. Write register 0xEF with value 0x02
46. Write register 0x11 with value 0x04
47. Write register 0x19 with value 0x45
48. Write register 0x1A with value 0x00
49. Write register 0x21 with value 0x50
50. Write register 0x22 with value 0x00
51. Write register 0x23 with value 0x3C
52. Write register 0x24 with value 0x00
53. Write register 0x27 with value 0x09
54. Write register 0x28 with value 0x00
55. Write register 0x2D with value 0x3C
56. Write register 0x2E with value 0x00
57. Write register 0xEF with value 0x00
58. Write register 0x05 with value 0x01
59. Write register 0x07 with value 0x02
60. Write register 0x0E with value 0xC0
61. Write register 0x32 with value 0x10
62. Write register 0x79 with value 0x01
63. Write register 0x7A with value 0x00
64. Write register 0x7B with value 0x02
65. Write register 0x7C with value 0x01
66. Write register 0x7F with value 0x02
67. Write register 0x80 with value 0x08
68. Write register 0x81 with value 0x00
69. Write register 0x82 with value 0x00
70. Write register 0x83 with value 0x00
71. Write register 0x84 with value 0x3B
72. Write register 0x85 with value 0x4F
73. Write register 0x93 with value 0x08
74. Write register 0x95 with value 0x02
75. Write register 0xA4 with value 0x0F
76. Write register 0xCD with value 0x20
77. Write register 0xCE with value 0x46
78. Write register 0xCF with value 0x10
79. Write register 0xD0 with value 0x14
80. Write register 0xD1 with value 0x00

81. Write register 0xD2 with value 0x03
82. Write register 0xD3 with value 0x14
83. Write register 0xD4 with value 0x00
84. Write register 0xD5 with value 0x03
85. Write register 0xD6 with value 0x14
86. Write register 0xD7 with value 0x00
87. Write register 0xD8 with value 0x03
88. Write register 0xD9 with value 0x14
89. Write register 0xDA with value 0x00
90. Write register 0xDB with value 0x03
91. Write register 0xDF with value 0x10
92. Write register 0xE1 with value 0x10
93. Write register 0xE2 with value 0x13
94. Write register 0xE3 with value 0x13
95. Write register 0xE4 with value 0x11
96. Write register 0xEF with value 0x02
97. Write register 0x7D with value 0x01
98. Write register 0xEF with value 0x00
99. Write register 0xE5 with value 0x07
100. Write register 0xE5 with value 0x03
101. Write register 0xE5 with value 0x01
102. Write register 0xE5 with value 0x00
103. Write register 0x09 with value 0x10
104. Write register 0x16 with value 0x3C
105. Write register 0x18 with value 0x02
106. Write register 0x1C with value 0x82
107. Write register 0x2F with value 0x44
108. Write register 0x37 with value 0x04
109. Write register 0x38 with value 0x06
110. Write register 0x3E with value 0x26
111. Write register 0x3F with value 0x81
112. Write register 0x55 with value 0x01
113. Write register 0x66 with value 0x04
114. Write register 0xEF with value 0x01
115. Write register 0x03 with value 0x00
116. Write register 0x04 with value 0x31
117. Write register 0x0A with value 0x00
118. Write register 0x0B with value 0x24
119. Write register 0x36 with value 0x00
120. Write register 0x37 with value 0x02
121. Write register 0x4D with value 0x02
122. Write register 0x54 with value 0x01
123. Write register 0x63 with value 0x06
124. Write register 0x6B with value 0x3E
125. Write register 0x6C with value 0x3E
126. Write register 0x70 with value 0x20
127. Write register 0x77 with value 0x09
128. Write register 0x79 with value 0x02
129. Write register 0x8A with value 0x50
130. Write register 0x8D with value 0x50
131. Write register 0xEF with value 0x02
132. Write register 0x02 with value 0xE1
133. Write register 0x03 with value 0x08
134. Write register 0x44 with value 0x01
135. Write register 0x45 with value 0xFF
136. Write register 0x47 with value 0xD0
137. Write register 0x5B with value 0x01
138. Write register 0x92 with value 0x04
139. Write register 0x93 with value 0x14
140. Write register 0xC3 with value 0x91
141. Write register 0xC4 with value 0x00
142. Write register 0xC5 with value 0x91
143. Write register 0xC6 with value 0x00
144. Write register 0xEF with value 0x00
145. Write register 0xEB with value 0x80
146. Write register 0x30 with value 0x01

8.2 Registers Access

The host may access register through I^2C interface. Refer to Section 6.0 for detail.

8.2.1 Registers Address Mapping

The sensor has two type of register assignment. They are register bank and register address mapping. Each register bank consists of 8 bits width address mapping (0x00 to 0xFF).

8.2.2 Register Bank Switching

The *Bank_Number* is the register bank location to perform the register bank switching. This bank register address is configured as common address for every register bank called non-bank register.

As similar address mapping register is applicable for every register bank, the host need to ensure the correct register bank switching prior perform any register read or write operation.

There are 4 banks for the sensor, which is Bank 0 to Bank 2 and Bank4.

- Bank 0: Write register 0xEF with value 0x00 to switch to bank 0.
- Bank 1: Write register 0xEF with value 0x01 to switch to bank 1
- Bank 2: Write register 0xEF with value 0x02 to switch to bank 2
- Bank 4: Write register 0xEF with value 0x04 to switch to bank 4

8.2.3 Register Update

The *update flag* is the control bit to make the register settings officially activated. It is recommended to configure as many settings as required before register update as the final step. Refer to Section 10.6 for all the relevant register or bit involved.

8.3 Continuous Mode

After initial setting (refer to Section 8.1.3), the sensor enters this mode by setting *R_TG_En* = 1. The sensor transmits image data through parallel interface.

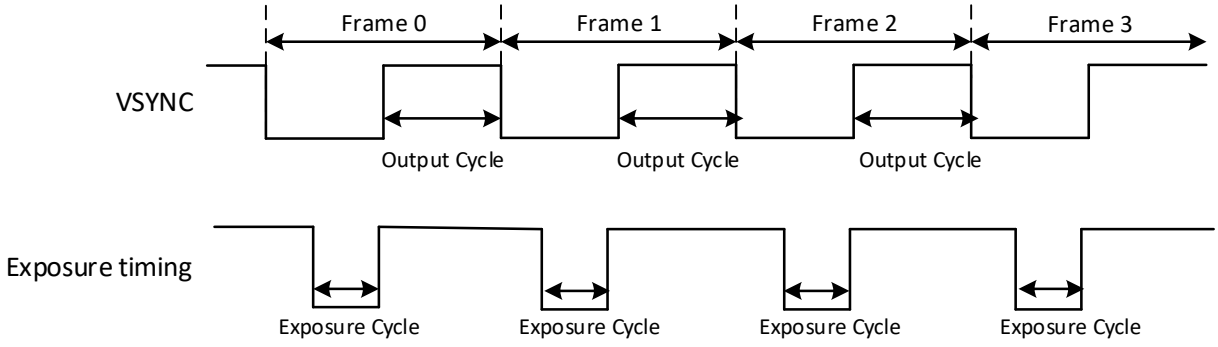


Figure 39. Continuous Mode Timing

8.4 Trigger Mode

8.4.1 Trigger Mode Timing

The sensor only outputs single one frame data when receiving of trigger command from the host. In Trigger Mode, the frame rate is determined by the host trigger command interval.

Under manual exposure control, the value of t_d shows the table.

Table 30. Delay Time from Trigger to Exposure

Parameter	Symbol	Min.	Typ.	Max.	Unit
Delay Time	t_d	1.11	1.78	4.45	ms

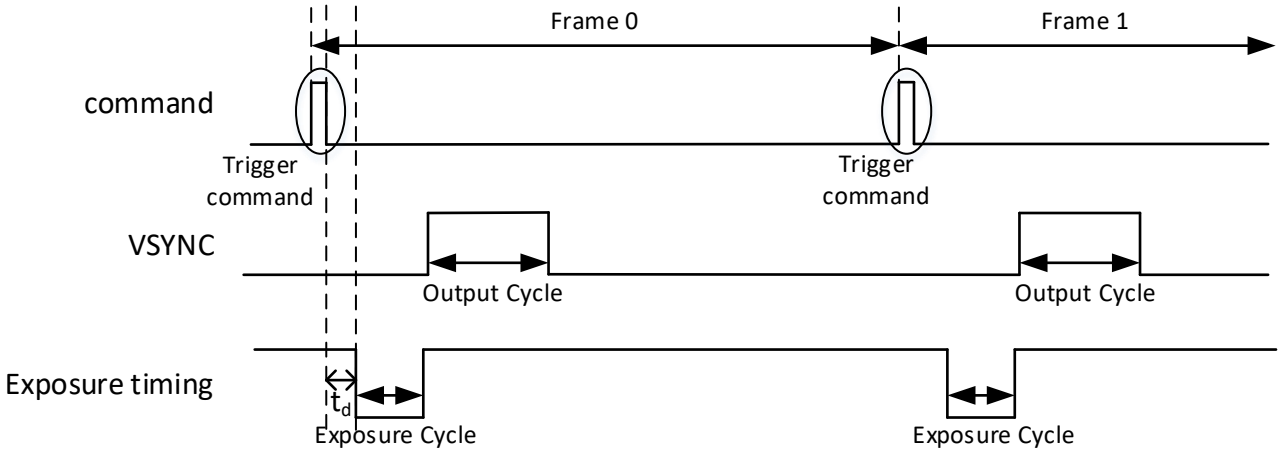


Figure 40. Trigger Mode Timing

The sensor enters Trigger mode settings as follow:

1. Write register 0xEF with value 0x00 //Switching to Register bank 0
2. Write register 0x30 with value 0x00 // *R_TG_En* = 0
3. Write register 0x31 with value 0x01 // *R_Trigger_En* = 1

The host set bank 0 register 0xEA with value 0x01 to perform trigger activity. Below is the command sequence

Write register 0xEA with value 0x01 // Trigger command

8.5 Motion Detection

With a fix background, the sensor adopts frame comparison for motion detection. The sensor compares the current image with reference image to calculate the differences of pixel luminous. If the number of pixels is larger than pixel number threshold, then output the motion detection interrupt signal.

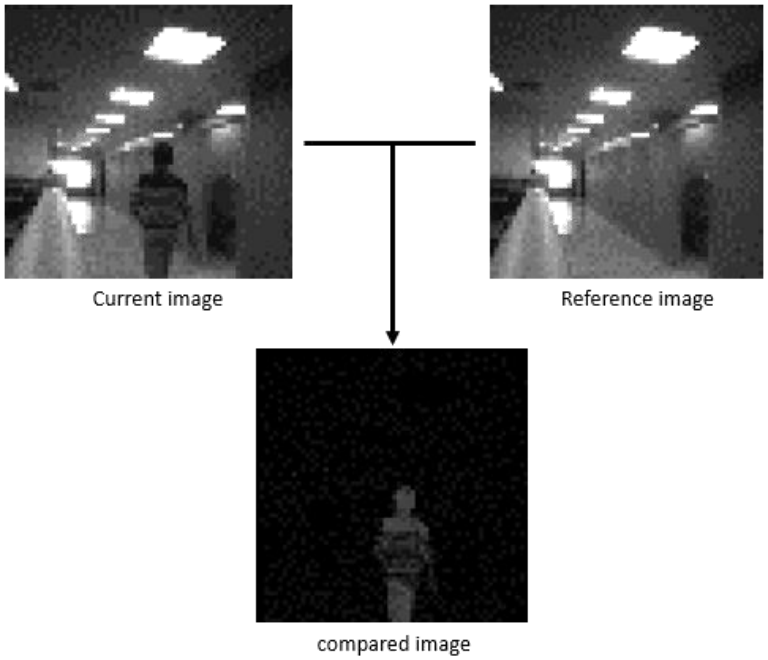


Figure 41. Motion Detection Working Fundamental

The user can configure maximum four specific detecting window area for motion detection. The window detection setup step as follows:

1. Set motion windows starting position and size by *R_WOI_HStart[n]*, *R_WOI_VStart[n]*, *R_WOI_HEnd[n]*, *R_WOI_Vend[n]*(n=1 to 4). Maximum can setup four motion windows.
2. Outside or inside of motion detection zone by configuring *R_WOI_InorEx[n]*(n=1 to 4)
3. Configure pixel count threshold *R_WOI1_Frame_Thd*[7:0], *R_WOI2_Frame_Thd*[7:0], *R_WOI3_Frame_Thd*[7:0] and *R_WOI4_Frame_Thd*[7:0]
4. Motion window function can be enabled or disabled by configuring *R_WOI_En[n]* (n=1 to 4).

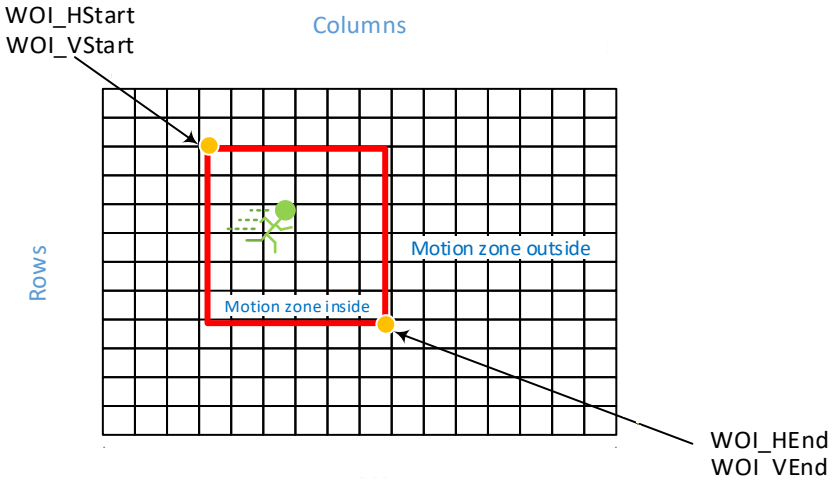


Figure 42. Motion Window

Output:

WOIn_Diff_cnt
WOIx_Motion (interrupt Status)
Frame_Diff_Pixel_Xmin[6:0]
Frame_Diff_Pixel_Xmax[6:0]
Frame_Diff_Pixel_Ymin[5:0]
Frame_Diff_Pixel_Ymax[5:0]

The operation process as follow:

1. If the current and previous frame pixel brightness difference is greater than the threshold, the motion pixel is counted, and saved in *WOI1_Diff_cnt*, *WOI2_Diff_cnt, WOI3_Diff_cnt and WOI4_Diff_cnt* registers.
2. The sensor generates interrupt signal when individual WOI motion pixels count greater than threshold (*R_WOIn_Frame_Thd*) and update the *WOIn_Motion* register. The host to read *WOIn_Motion* register to identify the WOI source of motion detection event.
3. The host can access *Frame_Diff_Pixel_Xmin, Frame_Diff_Pixel_Xmax, Frame_Diff_Pixel_Ymin* and *Frame_Diff_Pixel_Ymax* for motion active area.

8.6 GPIO Control

There are two GPIO pins for the sensor.

Table 31. GPIO Signals Description

Signal Name	Type	Ready Status	Description
GPIO1	I/O	Hi-Z	▪ External LED control signal ▪ Motion mode interrupt signal ▪ Frame synchronization signal ▪ SPI image output interrupt signal ▪ External clock input signal
GPIO2	I/O	Hi-Z	▪ Select I²C Slave ID. Refer to Section 6.2. ▪ External LED control signal

The GPIO1 can be assigned and selected for one out of five control signals. The GPIO1 can be configured according to application requirement through configuring *R_GPIO1_sel* register.

The GPIO2 is primarily used for bootstrap I²C slave ID selection which cannot be disabled. If necessary, GPIO2 can be implemented into other functions after power-on setup time, such as LED Control. The GPIO2 can be configured according to application requirement through configuring *R_GPIO2_sel* register.

For example, GPIO1 will be configured as an SPI image output interrupt when the sensor operates in SPI image output mode. If LED Control is still needed during SPI image output mode, it can be implemented through GPIO2.

Due to GPIO2 is configured to I²C slave ID selection and external LED control, do take note that the external LED control circuit must not interfering with the I²C slave ID detection. For more detail, please contact your PixArt local FAE for additional assistance.

- For external LED control signal, the following takes GPIO1 as an example,

  GPIO1 needs to be configured as output signal where *R_GPIO1_sel = 1* (external LEDs control), *T_GPIO1_OE* (1 for output enable) and *T_GPIO1_INL* (1 for input disable).

  When GPIO1 is assigned as external LED timing control pin and the GPIO1 synchronized with exposure time.

  The synchronized external LED control signal can be configured to equal or earlier than exposure time through *R_expo_LED_early* register. The host can use this signal to control external LED via GPIO1 pin.

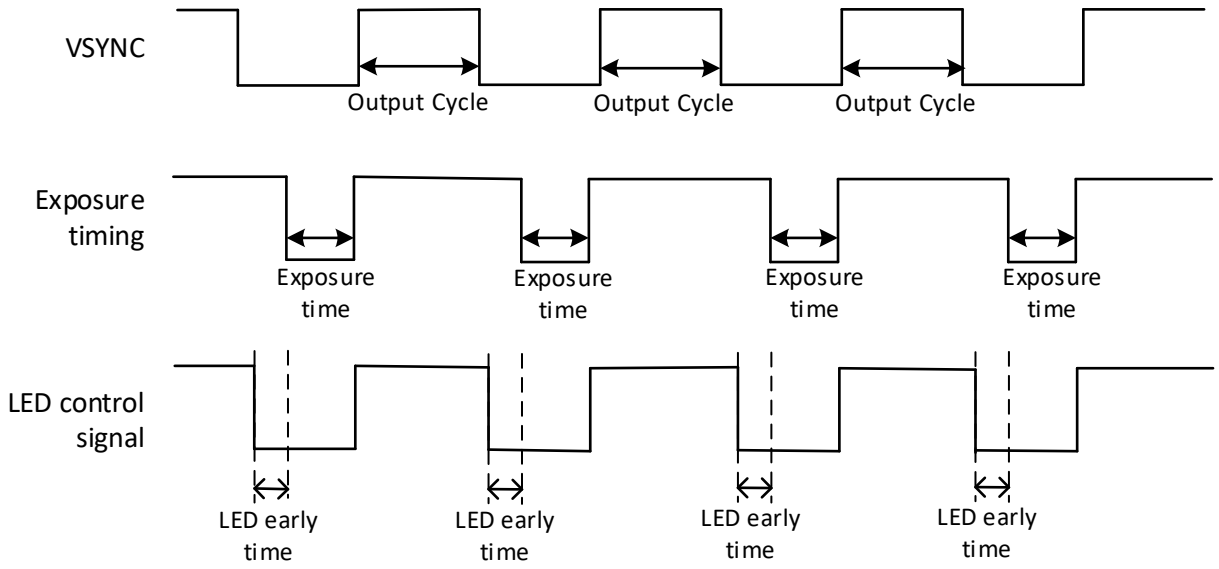


Figure 43. External LED Timing

- Motion mode interrupt signal

  GPIO1 need to be configured as output signal where *R_GPIO1_sel = 2* (motion mode interrupt), *T_GPIO1_OE* (1 for output enable) and *T_GPIO1_INL* (1 for input disable).

  When GPIO1 is assigned as motion mode interrupt pin and the timing shows as follow.

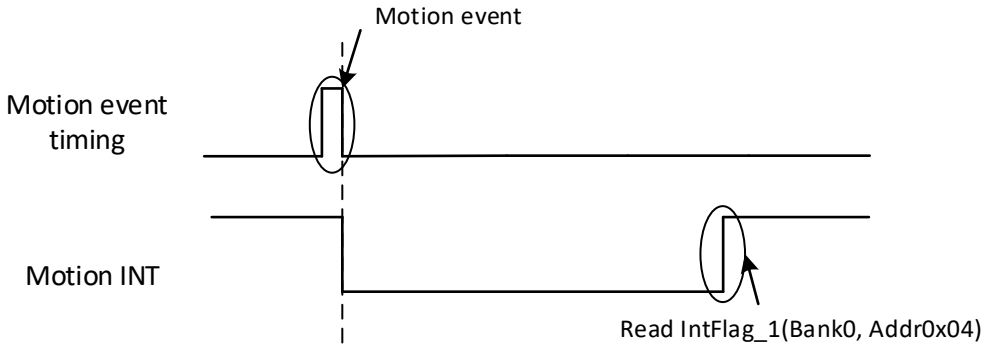


Figure 44. Motion INT Timing

Once motion interrupt is triggered, the GPIO1 pin is asserted until the *IntFlag_1* is read (*R_IntFlag_1_RdClr_En*= 1). The *IntFlag_1* register can be accessed to obtain the trigger area information. Refer to Section 8.5 for operation detail.

- Frame synchronization signal

  GPIO1 needs to be configured as output signal where *R_GPIO1_sel = 3* (frame synchronization signal), *T_GPIO1_OE* (1 for output enable) and *T_GPIO1_INL* (1 for input disable).

  When GPIO1 is assigned as frame synchronization signal and the timing refers to Section 8.7.

- SPI image output interrupt signal

  GPIO1 needs to be configured as output signal where *R_GPIO1_sel = 4* (SPI image output interrupt signal), *T_GPIO1_OE* (1 for output enable) and *T_GPIO1_INL* (1 for input disable).

  When GPIO1 is assigned as SPI image output interrupt signal and the timing refers to Section 7.3.

- External clock input signal

  GPIO1 needs to be configured as input signal where *T_GPIO1_OE* (0 for output disable) and *T_GPIO1_INL* (0 for input enable).

  When GPIO1 is assigned as external clock input signal and the timing refers to Section 5.5.

8.7 Frame Synchronization Control

The sensor design support multi-sensor frame synchronization architecture. Each sensor may configure to different I²C slave ID using GPIO2 strapping. The host may configure sensors independently to either master or slave sensor.

One host can support up to three sensors.

Setup Configuration

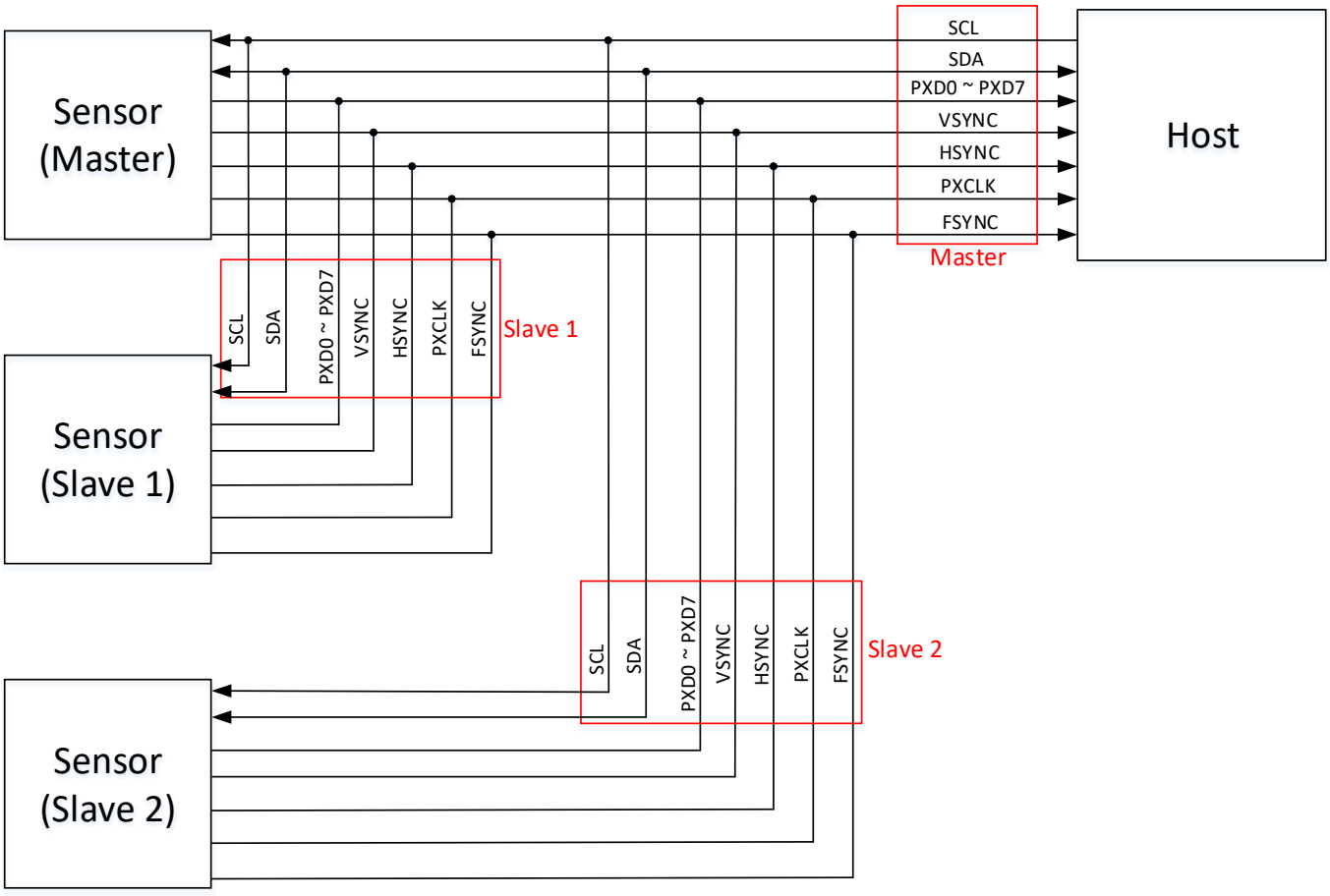


Figure 45. Multi-sensor Setup

The hardware setting steps as follows.

1. Set Master sensor GPIO2 as High state (pull-up) as Slave I²C ID: 0x25.
2. Set Slave1 sensor GPIO2 as Float state (floating) as Slave I²C ID: 0x35.
3. Set Slave2 sensor GPIO2 as Low state (pull-down) as Slave I²C ID: 0x40

The host must be set each sensor with respective setting. Then, set the initial setting by broadcast slave I²C ID (0x60) to each sensor at the same time. Finally, these sensors will start to output image.

8.7.1 Timing

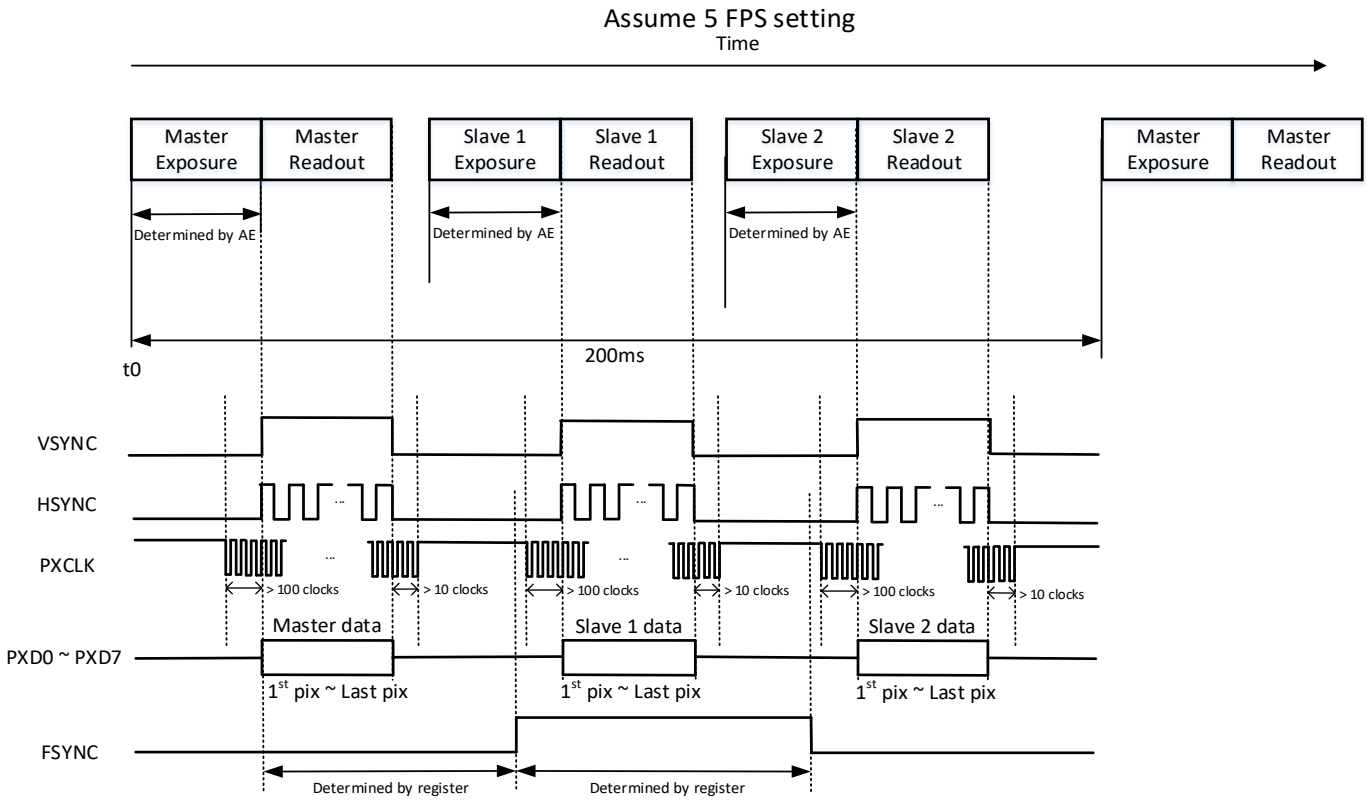


Figure 46. Multi-sensor Timing

8.7.2 Multi-sensor Setting

8.7.2.1 Master Sensor

1. Write register 0xEF with value 0x00
2. Write register 0x45 with value 0x44
3. Write register 0x07 with value 0x03
4. Write register 0x0E with value 0xC0
5. Write register 0x0C with value 0xC8
6. Write register 0x11 with value 0xC8
7. Write register 0x42 with value 0xC8
8. Write register 0x43 with value 0xC8
9. Write register 0x44 with value 0xC8
10. Write register 0xEF with value 0x04
11. Write register 0xD0 with value 0x23
12. Write register 0xD1 with value 0x0F
13. Write register 0xD2 with value 0x00
14. Write register 0xD3 with value 0x01
15. Write register 0xD4 with value 0xFF
16. Write register 0xD5 with value 0x01
17. Write register 0xEF with value 0x00
18. Write register 0xAD with value 0x10

8.7.2.2 Slave1 Sensor

1. Write register 0xEF with value 0x00
2. Write register 0x45 with value 0x44
3. Write register 0x0E with value 0x00
4. Write register 0x0C with value 0xC8
5. Write register 0x11 with value 0xC8
6. Write register 0x42 with value 0xC8
7. Write register 0x43 with value 0xC8
8. Write register 0x44 with value 0xC8
9. Write register 0xEF with value 0x01
10. Write register 0x28 with value 0x0D
11. Write register 0xEF with value 0x04
12. Write register 0xD0 with value 0x01
13. Write register 0xD1 with value 0x0F
14. Write register 0xD2 with value 0x00
15. Write register 0xD3 with value 0x01
16. Write register 0xD4 with value 0xFF
17. Write register 0xD5 with value 0x01
18. Write register 0xEF with value 0x00
19. Write register 0xAD with value 0x10

8.7.2.3 Slave2 Sensor

1. Write register 0xEF with value 0x00
2. Write register 0x45 with value 0x44
3. Write register 0x0E with value 0x00
4. Write register 0x0C with value 0xC8
5. Write register 0x11 with value 0xC8
6. Write register 0x42 with value 0xC8
7. Write register 0x43 with value 0xC8
8. Write register 0x44 with value 0xC8
9. Write register 0xEF with value 0x01
10. Write register 0x28 with value 0x0D
11. Write register 0xEF with value 0x04
12. Write register 0xD0 with value 0x05
13. Write register 0xD1 with value 0x0F
14. Write register 0xD2 with value 0x00
15. Write register 0xD3 with value 0x01
16. Write register 0xD4 with value 0xFF
17. Write register 0xD5 with value 0x01
18. Write register 0xEF with value 0x00
19. Write register 0xAD with value 0x10

8.7.2.4 Broadcast Setting

1. Write register 0xEF with value 0x00
2. Write register 0x1D with value 0x41
3. Write register 0x64 with value 0x01
4. Write register 0x12 with value 0x20
5. Write register 0xAF with value 0x31
6. Write register 0x69 with value 0x14
7. Write register 0x4C with value 0x00
8. Write register 0x4D with value 0x9F
9. Write register 0x4E with value 0x24
10. Write register 0x4F with value 0x00
11. Write register 0xEF with value 0x02
12. Write register 0x02 with value 0x64
13. Write register 0x03 with value 0x08
14. Write register 0xEF with value 0x04
15. Write register 0x2C with value 0xC6
16. Write register 0x2D with value 0x2D
17. Write register 0x2E with value 0x00
18. Write register 0x30 with value 0x31
19. Write register 0x31 with value 0x80
20. Write register 0x40 with value 0x1D
21. Write register 0x41 with value 0x00
22. Write register 0x42 with value 0xA0
23. Write register 0x43 with value 0x03
24. Write register 0x44 with value 0xF0
25. Write register 0x45 with value 0x00
26. Write register 0x46 with value 0x00
27. Write register 0x47 with value 0x00
28. Write register 0x48 with value 0x40
29. Write register 0x49 with value 0xCA
30. Write register 0x4A with value 0x22
31. Write register 0x4B with value 0x00
32. Write register 0x51 with value 0x1D
33. Write register 0x52 with value 0x00
34. Write register 0x53 with value 0xC0
35. Write register 0x54 with value 0xD4
36. Write register 0x55 with value 0x01
37. Write register 0x56 with value 0x00
38. Write register 0xEF with value 0x01
39. Write register 0xC4 with value 0x02
40. Write register 0xC6 with value 0x40
41. Write register 0xC7 with value 0x01
42. Write register 0xC8 with value 0xF0
43. Write register 0xC9 with value 0x00
44. Write register 0xEF with value 0x02
45. Write register 0x11 with value 0x03
46. Write register 0x19 with value 0xFC
47. Write register 0x1A with value 0x00
48. Write register 0x21 with value 0x40
49. Write register 0x22 with value 0x01
50. Write register 0x23 with value 0xF0
51. Write register 0x24 with value 0x00
52. Write register 0x27 with value 0x0C
53. Write register 0x28 with value 0x00
54. Write register 0x2D with value 0xF0
55. Write register 0x2E with value 0x00
56. Write register 0x56 with value 0x40
57. Write register 0x57 with value 0x01
58. Write register 0x58 with value 0xFE
59. Write register 0x59 with value 0x00
60. Write register 0xEF with value 0x01
61. Write register 0x33 with value 0x46
62. Write register 0x3B with value 0x30
63. Write register 0x40 with value 0x96
64. Write register 0xD9 with value 0x32
65. Write register 0xDB with value 0x64
66. Write register 0xDD with value 0x64
67. Write register 0xEF with value 0x02
68. Write register 0xA5 with value 0x00
69. Write register 0xA6 with value 0x96
70. Write register 0xEF with value 0x00
71. Write register 0x09 with value 0x10
72. Write register 0x18 with value 0x01
73. Write register 0x2F with value 0x44
74. Write register 0x37 with value 0x04
75. Write register 0x38 with value 0x06
76. Write register 0x3F with value 0x01
77. Write register 0x55 with value 0x01
78. Write register 0x66 with value 0x01
79. Write register 0xEF with value 0x01
80. Write register 0x03 with value 0x00

81. Write register 0x04 with value 0xAB
82. Write register 0x07 with value 0x02
83. Write register 0x0A with value 0x00
84. Write register 0x0B with value 0x40
85. Write register 0x0F with value 0x0B
86. Write register 0x11 with value 0x0A
87. Write register 0x13 with value 0x0C
88. Write register 0x16 with value 0x00
89. Write register 0x17 with value 0xA9
90. Write register 0x36 with value 0x00
91. Write register 0x37 with value 0x02
92. Write register 0x4D with value 0x02
93. Write register 0x56 with value 0xB8
94. Write register 0x57 with value 0x01
95. Write register 0x58 with value 0xB8
96. Write register 0x59 with value 0x01
97. Write register 0x62 with value 0x00
98. Write register 0x63 with value 0x06
99. Write register 0x69 with value 0x1C
100. Write register 0x6A with value 0x1D
101. Write register 0x6B with value 0x68
102. Write register 0x6C with value 0x67
103. Write register 0x76 with value 0x06
104. Write register 0x77 with value 0x09
105. Write register 0x78 with value 0x02
106. Write register 0x79 with value 0x03
107. Write register 0x84 with value 0x19
108. Write register 0x86 with value 0x14
109. Write register 0x87 with value 0x19
110. Write register 0x89 with value 0x14
111. Write register 0x8A with value 0x23
112. Write register 0x8C with value 0x1E
113. Write register 0x8D with value 0x23
114. Write register 0x8F with value 0x1E
115. Write register 0x9D with value 0x0A
116. Write register 0xA0 with value 0x00
117. Write register 0xD1 with value 0xC8
118. Write register 0xD2 with value 0x00
119. Write register 0xEF with value 0x02
120. Write register 0x92 with value 0x11
121. Write register 0x93 with value 0x01
122. Write register 0xC3 with value 0xC8
123. Write register 0xC4 with value 0x00
124. Write register 0xC5 with value 0xC8
125. Write register 0xC6 with value 0x00
126. Write register 0xD1 with value 0x45
127. Write register 0xEF with value 0x00
128. Write register 0xEB with value 0x80
129. Write register 0x30 with value 0x01

8.7.3 Exposure Time Limitation at Multi-sensor Mode

At multi-sensor mode, the maximum of exposure time is difference with single sensor. The formula refers to Section 9.2.2.

8.8 Related Register

- System Initialization

Usage	Name	Bank	Address
Check Part ID	*Part ID[7:0]* *Part ID[15:8]*	0x00	0x00 0x01

- Register Access

Usage	Name	Bank	Address
Bank Switching	*Bank_Number*	0x00	0xEF
Update Flag	*Update Flag*	0x00	0xEB

- Trigger Mode

Usage	Name	Bank	Address
Trigger Frame Number	*R_Trigger_FrameNum*	0x00	0x2E
TG Enable	*R_TG_En*	0x00	0x30
Trigger Function Enable	*R_Trigger_En*	0x00	0x31

- Motion Mode

Usage	Name	Bank	Address
WOI Enable	*R_WOI_Enable*	0x00	0x80
WOI Detect Zone	*R_WOI_detect_Zone*	0x00	0x81
WOI1 Position	*R_WOI_VStart1[5:0]* *R_WOI_HStart1[6:0]* *R_WOI_VEnd1[5:0]* *R_WOI_HEnd1[6:0]*	0x00	0x82 0x83 0x84 0x85
WOI2 Position	*R_WOI_VStart2[5:0]* *R_WOI_HStart2[6:0]* *R_WOI_VEnd2[5:0]* *R_WOI_HEnd2[6:0]*	0x00	0x86 0x87 0x88 0x89
WOI3 Position	*R_WOI_VStart3[5:0]* *R_WOI_HStart3[6:0]* *R_WOI_VEnd3[5:0]* *R_WOI_HEnd3[6:0]*	0x00	0x8A 0x8B 0x8C 0x8D
WOI4 Position	*R_WOI_VStart4[5:0]* *R_WOI_HStart4[6:0]* *R_WOI_VEnd4[5:0]* *R_WOI_HEnd4[6:0]*	0x00	0x8E 0x8F 0x90 0x91
WOIn_Motion	*WOIn_Motion*	0x00	0x94
WOI1 Difference count	*WOI1_Diff_cnt[7:0]* *WOI1_Diff_cnt[12:8]*	0x00	0x97 0x98
WOI2 Difference count	*WOI2_Diff_cnt[7:0]* *WOI2_Diff_cnt[12:8]*	0x00	0x99 0x9A
WOI3 Difference count	*WOI3_Diff_cnt[7:0]* *WOI3_Diff_cnt[12:8]*	0x00	0x9B 0x9C
WOI4 Difference count	*WOI4_Diff_cnt[7:0]* *WOI4_Diff_cnt[12:8]*	0x00	0x9D 0x9E
Frame Difference Pixel X position	*Frame_Diff_Pixel_Xmin[6:0]* *Frame_Diff_Pixel_Xmax[6:0]*	0x00	0x9F 0xA0
Frame Difference Pixel Y position	*Frame_Diff_Pixel_Ymin[5:0]* *Frame_Diff_Pixel_Ymax[5:0]*	0x00	0xA1 0xA2

Usage	Name	Bank	Address
WOI1 Frame Threshold	*R_WOI1_Frame_Thd[7:0]* *R_WOI1_Frame_Thd[12:8]*	0x00	0xD0 0xD1
WOI2 Frame Threshold	*R_WOI2_Frame_Thd[7:0]* *R_WOI2_Frame_Thd[12:8]*	0x00	0xD3 0xD4
WOI3 Frame Threshold	*R_WOI3_Frame_Thd[7:0]* *R_WOI3_Frame_Thd[12:8]*	0x00	0xD6 0xD7
WOI4 Frame Threshold	*R_WOI4_Frame_Thd[7:0]* *R_WOI4_Frame_Thd[12:8]*	0x00	0xD9 0xDA
IntFlag	*IntFlag_1[3:0]*	0x00	0x04
IntFlag Clear Enable	*R_IntFlag_1_RdClr_En*	0x00	0x05
Motion Detection Enable	*Rs_MotionDetection_EnH*	0x00	0x79
Interrupt Enable	*R_Int_1_En[3:0]*	0x00	0xA4
Interrupt Inverter	*R_Int_Inv*	0x00	0xA6

- GPIO

Usage	Name	Bank	Address
General-purpose I/O Control Register	*R_GPIO1_sel[7:0]* *R_GPIO2_sel[7:0]*	0x00	0x07 0x08
	GPIO control *GPIO1 control* *GPIO2 control*	0x00	0x0D 0x0E 0x0F
LED Control	*R_expo_LED_Manual_Mode_Sel [1:0]* *R_expo_LED_Period [3:0]* *R_expo_LED_early [7:0]* *R_expo_LED_polarity*	0x02	0x79 0x7A 0x7B 0x7C

- Frame Synchronization Control

Usage	Name	Bank	Address
Multi-sensor control	*R_Fsync_En* *R_Fsync_Master* *R_Fsync_SlaveLabel* *R_Fsync_SlaveNum*	0x04	0xD0
Fsync Output HoldTime	*R_Fsync_Output_HoldTime*	0x04	0xD1
Fsync Timing Control1	*R_Fsync_O_dly1[7:0]* *R_Fsync_O_dly1[15:8]*	0x04	0xD2 0xD3
Fsync Timing Control2	*R_Fsync_O_dly2[7:0]* *R_Fsync_O_dly2[15:8]*	0x04	0xD4 0xD5

9.0 Sensor Setting

9.1 Frame Rate Control

The *R_Frame_Time* register is used to adjust frame rate. Below is the formula:

Frame rate = (1÷*R_Frame_Time*) x (System Clock÷2)

For example:

R_Frame_Time = 100000, Frame rate = 120Hz
R_Frame_Time = 800000, Frame rate = 15Hz
R_Frame_Time = 12000000, Frame rate = 1Hz

where System Clock is default 24MHz for parallel image output interface and 12MHz for SPI image output interface.

The chip support AEC/AGC and the maximum exposure time needs to be adjusted accordingly along with frame rate setting.

- *R_Frame_Time* > 80000 (<150fps)

  For *R_Frame_Time* > 80000 (frame rate < 150fps), *R_Normal_PwrSv* set to 1 (write register 0x55 in Bank0 with value 0x00).

- 80000 ≥ *R_Frame_Time* > 67875 (150 fps to 177fps)

  For 80000 ≥ *R_Frame_Time* > 67875 (which is 150 fps to 177fps), *R_Normal_PwrSv* set to 0 (write register 0x55 in Bank0 with value 0x00).

The following is an example to show the step to change the frame rate for 160fps.

1. Write 0xEF with value 0x00 //switch to bank0
2. Write 0x4C with value 0xF8 //write *R_Frame_Time*[7:0] for 160fps
3. Write 0x4D with value 0x24 //write *R_Frame_Time*[15:8] for 160fps
4. Write 0x4E with value 0x01 //write *R_Frame_Time*[23:16] for 160fps
5. Write 0x4F with value 0x00 //write *R_Frame_Time*[27:24] for 160fps
6. Write 0x55 with value 0x00 //disable normal power saving
7. Write 0xEF with value 0x04 //switch to bank4
8. Write 0x48 with value 0xE8 //wirte *R_AE_MaxExpo*[7:0] for 160fps, must < *R_Frame_Time*-10000
9. Write 0x49 with value 0xFD //wirte *R_AE_MaxExpo*[15:8] for 160fps,
10. Write 0x4A with value 0x00 //wirte *R_AE_MaxExpo*[23:16] for 160fps,
11. Write 0x4B with value 0x00 //wirte *R_AE_MaxExop*[27:24] for 160fps,
12. Write 0xEF with value 0x00 //switch to bank0
13. Write 0xEB with value 0x80 //*update flag*

- *R_Frame_Time* ≤ 67875 (≥177fps)

  For *R_Frame_Time* ≤67875 (frame rate ≥177fps), *R_Normal_PwrSv* set to 0 (write register 0x55 in Bank0 with value 0x00) with at least 10ms delay time after initial setting.

  The following is an example to show the step to change the frame rate for 180fps.

  1. Write 0xEF with value 0x00 //switch to bank0
  2. Write 0x4C with value 0x6A //write *R_Frame_Time*[7:0] for 180fps
  3. Write 0x4D with value 0x04 //write *R_Frame_Time*[15:8] for 180fps
  4. Write 0x4E with value 0x01 //write *R_Frame_Time*[23:16] for 180fps
  5. Write 0x4F with value 0x00 //write *R_Frame_Time*[27:24] for 180fps
  6. Write 0xEF with value 0x04 //switch to bank4
  7. Write 0x48 with value 0xE2 //wirte *R_AE_MaxExpo*[7:0] for 180fps, must < *R_Frame_Time*-10000
  8. Write 0x49 with value 0xF0 //wirte *R_AE_MaxExpo*[15:8] for 180fps,
  9. Write 0x4A with value 0x00 //wirte *R_AE_MaxExpo*[23:16] for 180fps,
  10. Write 0x4B with value 0x00 //wirte *R_AE_MaxExop*[27:24] for 180fps,
  11. Write 0xEF with value 0x00 //switch to bank0
  12. Write 0xEB with value 0x80 //*update flag*
  13. Write 0x30 with value 0x01 //enable TG
  14. delay for at least 10ms
  15. Write 0xEF with value 0x00 //switch to bank0
  16. Write 0x55 with value 0x00 //disable *R_Normal_PwrSv*[0]

Note: *R_Frame_Time* value must be greater than exposure time register (*R_AE_MaxExpo*/*R_AE_Expo_manual*).

9.2 Auto Analog Gain Control/ Auto Exposure Time Control

The AE window and AE active range need to be configured before enable AEC/AGC function. Here are the related register and description as shown below.

Parameter	Description	Recommended Value
R_AE_Start_div4_X	Horizontal Start point of AE Window	0
R_AE_Start_div4_Y	Vertical Start point of AE Window	0
R_AE_Size_div4_X	Horizontal X-Axis Distance/4 of AE window	80
R_AE_Size_div4_Y	Vertical Y-Axis Distance/4 of AE Window	60
R_Ytar8bit (Ytarget)	AE converge target intensity of brightness.	128
R_AE_LockRange_In	If AE window bright intensity is (R_Ytar8bit ± R_AE_LockRange_In), then AE convergence.	8
R_AE_LockRange_Out_LB	If AE window bright intensity smaller than (R_Ytar8bit - R_AE_LockRange_Out_LB), the image bright intensity will be adjusted.	16
R_AE_LockRange_Out_UB	If AE window bright intensity greater than (R_Ytar8bit + R_AE_LockRange_Out_UB), the image bright intensity will be adjusted.	16
R_AE_MaxExpo	Maximum exposure time based on AE window size and Frame rate	790000(15 FPS)
R_AE_MinExpo	Minimum exposure time	240
R_AE_MaxGain	Maximum gain	464
R_AE_MinGain	Minimum gain	29
AE_Total_Gain	Analog gain value of the present image	
Reg_ExpPxclkNum	Exposure time value of the present image	

9.2.1 AE Window

The AEC algorithm allows user to define the AE activity window which includes

1. AE window start position: *R_AE_Start_div4_X, R_AE_Start_div4_Y*.
2. AE window size (X-Axis/ 4 and Y-Axis/ 4): *R_AE_Size_div4_X, R_AE_Size_div4_Y*.

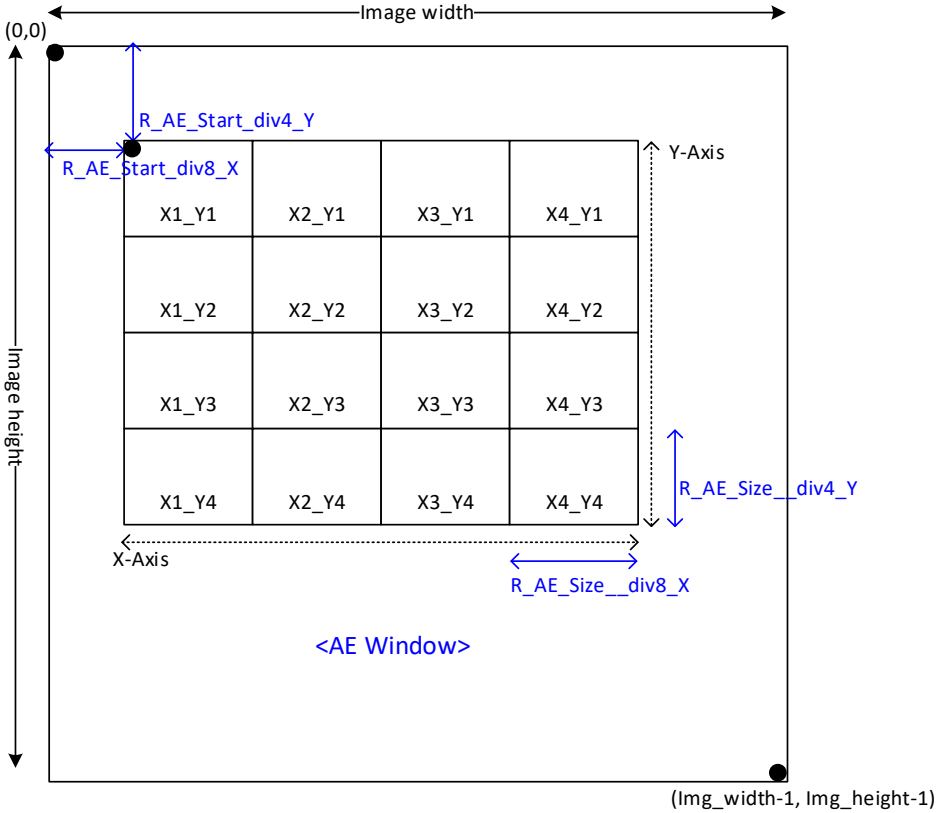


Figure 47. AE Window

9.2.2 Auto Exposure Control Range

The sensor can self-optimize image exposure time through auto exposure control function enable. The host can input *R_AE_MaxExpo* and *R_AE_MinExpo* to limit the auto exposure time control range. The exposure time range is based on frame rate.

The formula for calculating the maximum exposure time as follows:

R_AE_MaxExpo = *R_Frame_Time* -10000
Convert to second from *R_AE_MaxExpo*:
Max. time= *R_AE_MaxExpo* ÷ (System Clock ÷ 2)
where System Clock is default 24MHz for parallel image output interface and 12MHz for SPI image output interface.

For example:

R_AE_MaxExpo = 790000, Max. Exposure time: 65.83 ms

Note:

1. After setting *R_AE_MaxExpo, R_AE_MinExpo* or *R_AE_Expo_manual* register value for Exposure time control, set *update flag* to activate.
2. *R_AE_MaxExpo, R_AE_MinExpo* or *R_AE_Expo_manual* value must be at least 240 and not greater than frame time.

The formula for calculating the maximum exposure time at multi-sensor mode is as follows:

If *R_Frame_Time* ≥ 1560000, the *R_AE_MaxExpo* = R_Frame_Time x 0.95
If *R_Frame_Time* < 1560000, the *R_AE_MaxExpo* = R_Frame_Time – 78000

9.2.3 Auto Gain Control Range

The sensor can self-optimize image brightness through auto-gain control function enable. The host can input *R_AE_MaxGain* and *R_AE_MinGain* to limit the sensor auto gain control range. The analog gain range is derived from *R_AE_MaxGain* and *R_AE_MinGain* divided by 29.

For example, to calculation:

R_AE_MaxGain= 464, the maximum analog gain is 16x
R_AE_MinGain= 29, the minimum analog gain is 1x

Notes:

1. *R_AE_MaxGain* gain value not greater than 464.
2. *R_AE_MinGain* value must be at least 29.

9.2.4 AE Converge Range

Figure 48 shows an illustration of the AE active range. The AE converging steps as follow:

1. Configure *R_Ytar8bit* to input AE target intensity (Ytarget).
2. Sensor captures AE window intensity (Ycap8bit).
3. Sensor compares Ytarget and Ycap8bit to decide for AE activation.
4. If AE activated, the gain and exposure value will adjust automatically until Ycap8bit fall in "Ytarget ± *R_AE_LockRange_In"* range. Then, AE is converged.
5. When AE is converged, the Gain and Exposure value is kept until Ycap8bit value less than "Ytarget - R_AE_LockRange_Out_LB of value or greater than Ytarget + R_AE_LockRange_Out_UB of value. Then, AE is not converged and activities continues.
6. Repeat Step 2 to 5 after AE is enabled.

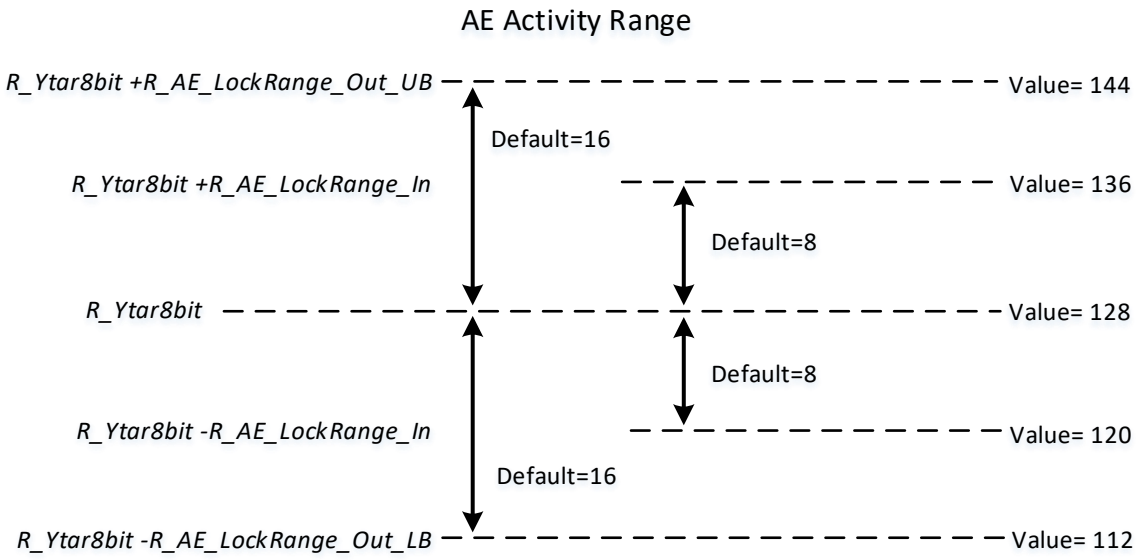


Figure 48. AE Activity Range

9.3 Manual Exposure Time and Analog Gain Control

For manual exposure time and analog gain control, step in sequence as follow

1. The host may disable Auto Exposure time and Auto Analog gain through clearing *R_AE_EnH* (= 0). The sensor may continue operate based on previous Exposure and Gain value.
2. Setup the manual gain and exposure time control value
   - Manual Exposure Time Control

     Formula:

     Exposure Time= *R_AE_Expo_manual* ÷ (System Clock÷2)

     where System Clock is default 24MHz for parallel image output interface and 12MHz for SPI image output interface.

     For example:

     R_AE_Expo_manual = 790000, Exposure time: 65.83 ms for parallel image output interface

   - Manual Gain Control

     The analog gain is derived from *R_AE_Gain_manual* value divided by 29.

     For example:
     R_AE_Gain_manual = 232, Manual Analog Gain= 8x

3. Set *R_AE_manual_En*= 1 and *R_AE_EnH* = 1 to enable manual exposure time and analog gain control.
4. Set Update flag to activate.

The following is an example to show the step for changing the exposure time control from auto control to manual control,

1. Write 0xEF register with value 0x04 //switch to bank4
2. Write 0x30 register with value 0x30 //set *R_AE_EnH*[0]=0 to disable the AEC/AGC engine and keep the //exposure time and gain value of the latest output of the AEC/AGC //engine
3. Write 0x53 register with value 0xA0 //set manual exposure time as e.g. 100000
4. Write 0x54 register with value 0x86 //set manual exposure time as e.g. 100000
5. Write 0x55 register with value 0x01 //set manual exposure time as e.g. 100000
6. Write 0x56 register with value 0x00 //set manual exposure time as e.g. 100000
7. Write 0xEF register with value 0x00 //switch to bank0
8. Write 0xEB register with value 0x80 //*update flag*
9. Write 0xEF register with value 0x04 //switch to bank4
10. Write 0x30 register with value 0x33 //enable AEC/AGC engine and switch to manual exposure control //simultaneously

Note: *R_AE_Gain_manual* gain value not greater than 464, and must be at least 29.

9.4 Related Register

- Frame Rate Control

Usage	Name	Bank	Address
Frame_Time	*R_Frame_Time[7:0]*	0x00	0x4C
	R_Frame_Time[15:8]		0x4D
	R_Frame_Time[23:16]		0x4E
	R_Frame_Time[27:24]		0x4F

- Power Saving

Usage	Name	Bank	Address
Normal_PwrSv	*Normal_PwrSv[0]*	0x00	0x55

- Auto Gain Control/ Auto Exposure Control

Usage	Name	Bank	Address
AE Window Control Register	*R_AE_Start_div4_X*	0x04	0x38
	R_AE_Start_div4_Y		0x39
	R_AE_Size_div4_X	0x04	0x3A
	R_AE_Size_div4_Y		0x3B
AE Function Enable Control	*AE Enable Control*	0x04	0x30
AE Activity Range Register	*R_Ytar8bit (Ytarget)*	0x04	0x31
	R_AE_LockRange_In	0x04	0x32
	R_AE_LockRange_Out_LB	0x04	0x33
	R_AE_LockRange_Out_UB		0x34
Auto Exposure Time Range Register	*R_AE_MinExpo [7:0]*	0x04	0x44
	R_AE_MinExpo [15:8]		0x45
	R_AE_MinExpo [23:16]		0x46
	R_AE_MinExpo [27:24]		0x47
	R_AE_MaxExpo [7:0]	0x04	0x48
	R_AE_MaxExpo [15:8]		0x49
	R_AE_MaxExpo [23:16]		0x4A
	R_AE_MaxExpo [27:24]		0x4B
Auto Gain Range Register	*R_AE_MinGain [7:0]*	0x04	0x40
	R_AE_MinGain [10:8]		0x41
	R_AE_MaxGain [7:0]		0x42
	R_AE_MaxGain [10:8]		0x43
AEC/AGC Present Value Read Register	*AE_Total_Gain[7:0]*	0x04	0xA5
	AE_Total_Gain[10:8]		0xA6
	Reg_ExpPxclkNum[7:0]	0x04	0xA7
	Reg_ExpPxclkNum[15:8]		0xA8
	Reg_ExpPxclkNum[23:16]		0xA9
	Reg_ExpPxclkNum[27:24]		0xAA

- Manual Exposure Time and Analog Gain Control

Usage	Name	Bank	Address
Gain Manual Control	*R_AE_Gain_manual[7:0]* *R_AE_Gain_manual[10:8]*	0x04	0x51 0x52
Exposure Manual Control	*R_AE_Expo_manual [7:0]* *R_AE_Expo_manual [15:8]* *R_AE_Expo_manual [23:16]* *R_AE_Expo_manual [27:24]*	0x04	0x53 0x54 0x55 0x56

10.0 Image Signal Processing Function

10.1 Mirror and Flip Function

This sensor can perform mirror (H-flip) and flip (V-flip) function which respectively reverse the sensor data read out order horizontally and vertically.

Below is the example of mirror and flip function.

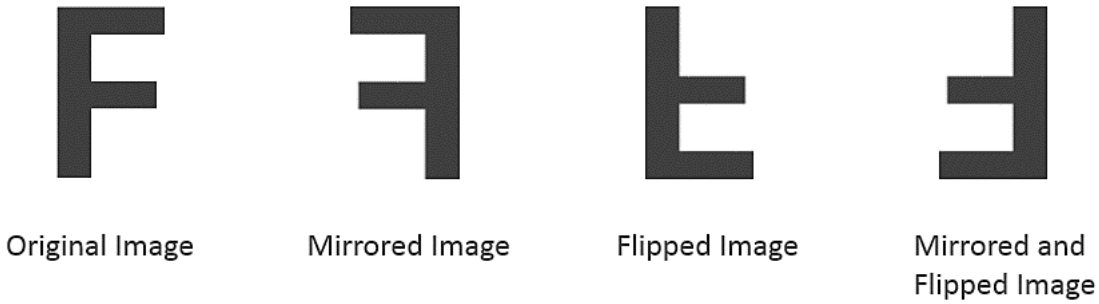


Figure 49. Mirror and Flip Samples

10.1.1 Original Setting

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x00
3. Write register 0xEF with value 0x01
4. Write register 0xC2 with value 0x00
5. Write register 0xCB with value 0x04
6. Write register 0xCE with value 0x00
7. Write register 0xEF with value 0x02
8. Write register 0xD9 with value 0x00
9. Write register 0xEF with value 0x00
10. Write register 0xEB with value 0x80
11. Write register 0x30 with value 0x01

10.1.2 Mirror Setting

1. Write register 0xEF with value 0x00
2. Write register 0x09 with value 0x02
3. Write register 0xEF with value 0x02
4. Write register 0xD9 with value 0x02
5. Write register 0xEF with value 0x00
6. Write register 0xEB with value 0x80
7. Write register 0x30 with value 0x01

10.1.3 Flip Setting

1. Write register 0xEF with value 0x01
2. Write register 0xC2 with value 0xF7
3. Write register 0xCB with value 0xF3
4. Write register 0xCE with value 0x04
5. Write register 0xEF with value 0x00
6. Write register 0xEB with value 0x80
7. Write register 0x30 with value 0x01

10.1.4 Mirrored and Flipped

When both mirrored and flipped are enabled at the same time, config both Mirror and Flip Setting in any sequence.

10.2 Skip

The sensor can perform Digital skip function where covers both horizontal and vertical directions. Figure 50 is the example of skip function. It performs 2x skip (in both horizontal and vertical directions) which depends on different image interfaces and settings.

The analog skip function will be assigned based on the initial settings.

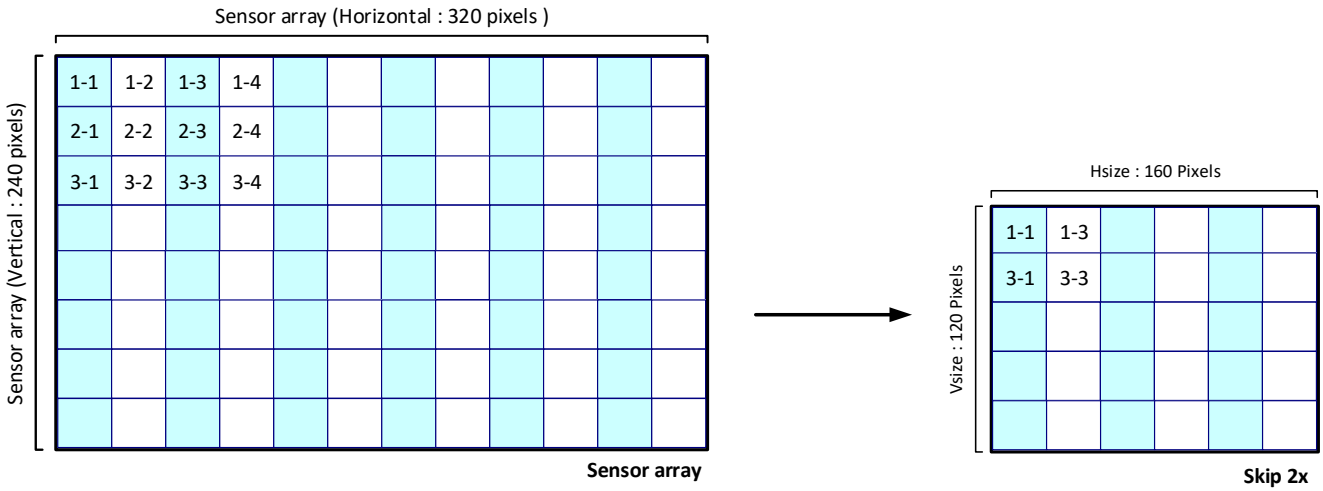


Figure 50. Example of Skip Function

10.3 Average

Average in general will combine the information of adjacent pixel into a resulting information depending on average mode. That will in any case lead to a reduced resolution by the factor of average while maintaining the same field of view. Average is usually designed for increasing the pixel's signal-to-noise ratio (SNR). This builds the source pixel average information to the result pixel with the advantage of reducing noise in the result information.

The analog average function will be assigned based on the initial settings. Figure 51 is the example of average function. It performs 2x average in both horizontal and vertical directions depend on different image interface and setting.

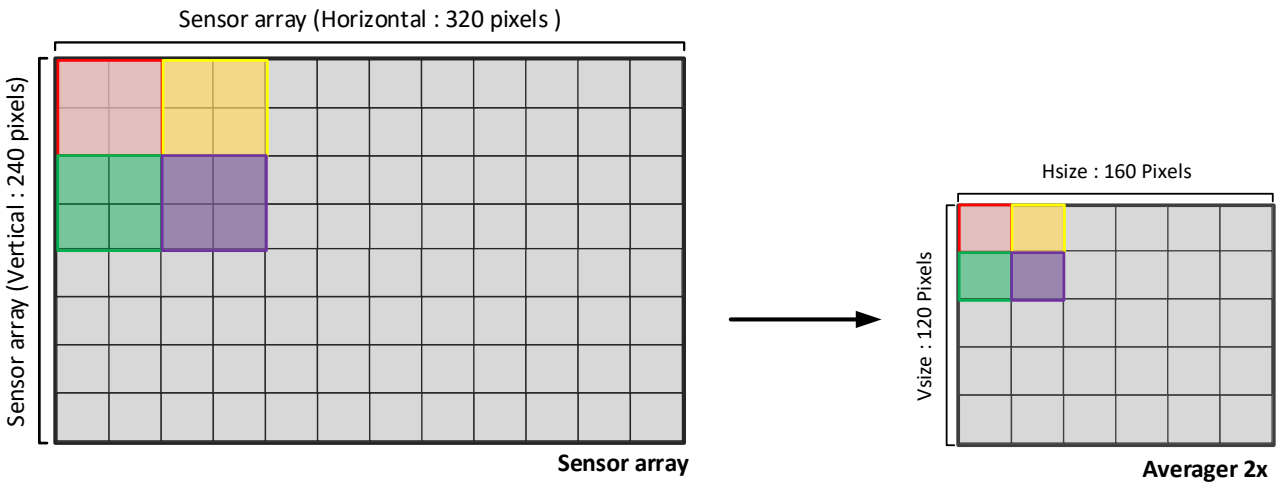


Figure 51. Example of Average Function

10.4 Image WOI (Window of Interest)

The sensor can perform image Window of Interest (WOI) setting function. It allows the host to set predefined WOI regions of active sensing region. This WOI setting is benefiting the sensor power saving and image data content reduction for transmission.

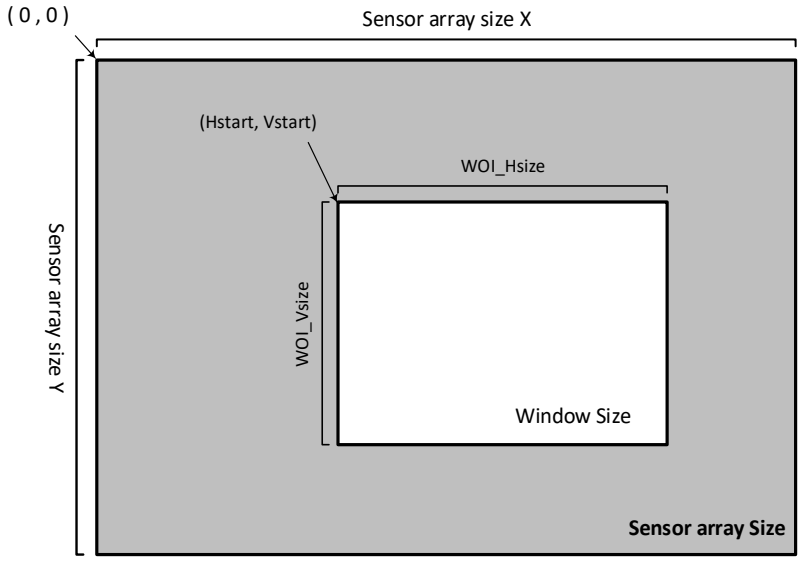


Figure 52. WOI Framing

The WOI area is defined through configuring four registers, *R_WOI_HSize*, *R_WOI_VSize*, *R_WOI_HStart* , and *R_WOI_VStart*. The area within the window is the interested area.

After set the related parameters, do set *R_WOI_EnH*= 1 to enable the WOI function. Then, set *update flag* to activate.

When WOI is enabled, the non-interested area (outside the WOI area) will be masked off and output will be ignored. The WOI enable / disable will not affect the conversion timing.

10.5 Test Pattern

User can write corresponding setting to generate test pattern.

10.5.1 Ramp Mode

The sensor can be configured to generate test pattern. The setting as follows:

1. Write register 0xEF with value 0x04
2. Write register 0x00 with value 0x01
3. Write register 0x0A with value 0x04

Figure 53. Test Pattern

10.6 Related Register

- Flip Control Register

Usage	Name	Bank	Address
Mirror Control	*Mirror*	0x00	0x09
Flip Control	*Flip*	0x01	0xCE
Line Start Position	*R_VsettleStart [7:0]* *R_VsettleStart [8]* *R_VStart [7:0]* *R_VStart [8]*	0x01	0xC2 0xC3 0xCB 0xCC

- Window of Interest (WOI)

Usage	Name	Bank	Address
WOI_EnH	*R_WOI_EnH*	0x02	0x55
WOI_HSize	*R_WOI_HSize[7:0]* *R_WOI_HSize[9:8]*	0x02	0x21 0x22
WOI_VSize	*R_WOI_VSize[7:0]* *R_WOI_VSize[8]*	0x02	0x23 0x24
WOI_HStart	*R_WOI_HStart[7:0]* *R_WOI_HStart[9:8]*	0x02	0x25 0x26
WOI_VStart	*R_WOI_VStart[7:0]* *R_WOI_VStart[8]*	0x02	0x27 0x28

11.0 Registers

11.1 Register Map

Table 32. Non-Bank Registers

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0xEF		Bank_Number	-	W	-	0x00

Table 33. Bank0 Registers

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0x00	-	PartID[7:0]	-	R	-	0x20
0x01	-	PartID[15:8]	-	R	-	0x79
0x04	Bit [3:0]	IntFlag_1	-	R/W	0	0x00
0x05	Bit [0]	R_IntFlag_1_RdClr_En	-	R/W	0	0x00
0x07	-	R_GPIO1_sel	-	R/W	-	0x00
0x08	-	R_GPIO2_sel	-	R/W	-	0x00
0x09	Bit [4]	R_HFLIP2	-	R/W	1	0x10
	Bit [1]	R_HFLIP1	-	R/W	0	
0x0D	-	GPIO control	-	R/W	-	0x00
	Bit [5]	AD_GPIO2	-	R	0	
	Bit [4]	AD_GPIO1	-		0	
	Bit [1]	R_GPIO2_O	-	R/W	0	
	Bit [0]	R_GPIO1_O	-		0	
0x0E	-	GPIO1 control	-	R/W	-	0x40
	Bit [7]	T_GPIO1_OE	-		0	
	Bit [6]	T_GPIO1_INL	-		1	
	Bit [5]	T_GPIO1_IDDQ	-		0	
	Bit [4]	T_GPIO1_SR	-		0	
	Bit [3:2]	T_GPIO1_OPDRV[1:0]	-		0	
	Bit [1]	T_GPIO1_PD	-		0	
	Bit [0]	T_GPIO1_PU	-		0	
0x0F	-	GPIO2 control	-	R/W	-	0x40
	Bit [7]	T_GPIO2_OE	-		0	
	Bit [6]	T_GPIO2_INL	-		1	
	Bit [5]	T_GPIO2_IDDQ	-		0	
	Bit [4]	T_GPIO2_SR	-		0	
	Bit [3:2]	T_GPIO2_OPDRV[1:0]	-		0	
	Bit [1]	T_GPIO2_PD	-		0	
	Bit [0]	T_GPIO2_PU	-		0	
0x26	-	External Clock Function 1	-	R/W	-	0x0A

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
	Bit [6:4]	T_spll_predivider[8:6]	-		0	
0x27	-	External Clock Function 1	-	R/W	-	0x41
	Bit [5:0]	T_spll_predivider[5:0]	-		1	
0x29	-	External Clock Function 2	-	R/W	-	0x64
	Bit [5:0]	T_spll_postdivider[5:0]	-		36	
0x2A	-	External Clock Function 2	-	R/W	-	0x10
	Bit [6:4]	T_spll_postdivider[8:6]	-		1	
0x2B	-	External Clock Function 3	-	R/W	-	0x03
	Bit [1]	T_spll_refsel	-		1	
	Bit [0]	T_spll_clock	-		1	
0x2E	-	R_Trigger_FrameNum[7:0]	-	R/W	-	0x01
0x30	Bit [0]	R_TG_En	-	R/W	0	0x00
0x31	Bit [0]	R_Trigger_En	-	R/W	0	0x00
0x36	-	External Clock Function 4	-	R/W	-	0x02
	Bit [1:0]	B_spll_EnH[1:0]	-		2	
0x4C	-	R_Frame_Time[7:0]	-	R/W	-	0x40
0x4D	-	R_Frame_Time[15:8]	-	R/W	-	0x0D
0x4E	-	R_Frame_Time[23:16]	-	R/W	-	0x03
0x4F	Bit [3:0]	R_Frame_Time[27:24]	-	R/W	0	0x00
0x79	Bit [0]	Rs_MotionDetection_EnH	-	R/W	0	0x00
0x80	-	R_WOI_Enable	-	R/W	-	0x00
	Bit [3]	R_WOI_En1	-		0	
	Bit [2]	R_WOI_En2	-		0	
	Bit [1]	R_WOI_En3	-		0	
	Bit [0]	R_WOI_En4	-		0	
0x81	-	R_WOI_detect_Zone	-	R/W	-	0x00
	Bit [3]	R_WOI_InorEx1	-		0	
	Bit [2]	R_WOI_InorEx2	-		0	
	Bit [1]	R_WOI_InorEx3	-		0	
	Bit [0]	R_WOI_InorEx4	-		0	
0x82	Bit [5:0]	R_WOI_VStart1[5:0]	-	R/W	0	0x00
0x83	Bit [6:0]	R_WOI_HStart1[6:0]	-	R/W	0	0x00
0x84	Bit [5:0]	R_WOI_VEnd1[5:0]	-	R/W	0	0x00
0x85	Bit [6:0]	R_WOI_HEnd1[6:0]	-	R/W	0	0x00
0x86	Bit [5:0]	R_WOI_VStart2[5:0]	-	R/W	0	0x00
0x87	Bit [6:0]	R_WOI_HStart2[6:0]	-	R/W	0	0x00
0x88	Bit [5:0]	R_WOI_VEnd2[5:0]	-	R/W	0	0x00
0x89	Bit [6:0]	R_WOI_HEnd2[6:0]	-	R/W	0	0x00
0x8A	Bit [5:0]	R_WOI_VStart3[5:0]	-	R/W	0	0x00
0x8B	Bit [6:0]	R_WOI_HStart3[6:0]	-	R/W	0	0x00
0x8C	Bit [5:0]	R_WOI_VEnd3[5:0]	-	R/W	0	0x00

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0x8D	Bit [6:0]	R_WOI_HEnd3[6:0]	-	R/W	0	0x00
0x8E	Bit [5:0]	R_WOI_VStart4[5:0]	-	R/W	0	0x00
0x8F	Bit [6:0]	R_WOI_HStart4[6:0]	-	R/W	0	0x00
0x90	Bit [5:0]	R_WOI_VEnd4[5:0]	-	R/W	0	0x00
0x91	Bit [6:0]	R_WOI_HEnd4[6:0]	-	R/W	0	0x00
0x94	-	WOIn_Motion	-	R	-	0x00
	Bit [3]	WOI1_Motion	-		0	
	Bit [2]	WOI2_Motion	-		0	
	Bit [1]	WOI3_Motion	-		0	
	Bit [0]	WOI4_Motion	-		0	
0x97	-	WOI1_Diff_cnt[7:0]	-	R	-	0x00
0x98	Bit [3:0]	WOI1_Diff_cnt[12:8]	-	R	0	0x00
0x99	-	WOI2_Diff_cnt[7:0]	-	R	-	0x00
0x9A	Bit [3:0]	WOI2_Diff_cnt[12:8]	-	R	0	0x00
0x9B	-	WOI3_Diff_cnt[7:0]	-	R	-	0x00
0x9C	Bit [3:0]	WOI3_Diff_cnt[12:8]	-	R	0	0x00
0x9D	-	WOI4_Diff_cnt[7:0]	-	R	-	0x00
0x9E	Bit [3:0]	WOI4_Diff_cnt[12:8]	-	R	0	0x00
0x9F	Bit [6:0]	Frame_Diff_Pixel_Xmin[6:0]	-	R	0	0x00
0xA0	Bit [6:0]	Frame_Diff_Pixel_Xmax[6:0]	-	R	0	0x00
0xA1	Bit [5:0]	Frame_Diff_Pixel_Ymin[5:0]	-	R	0	0x00
0xA2	Bit [5:0]	Frame_Diff_Pixel_Ymax[5:0]	-	R	0	0x00
0xA4	-	R_Int_1_En[7:0]	-	R/W	-	0x00
0xA6	Bit [0]	R_Int_Inv	-	R/W	0	0x00
0xAF	-	Parallel Interface Polarity	-	R/W		0x01
	Bit [6]	R_Parallel_Pxclk_Inv	-		0	
	Bit [5]	R_Parallel_Hsync_Inv	-		0	
	Bit [4]	R_Parallel_Vsync_Inv	-		0	
0xD0	-	R_WOI1_Frame_Thd[7:0]	-	R/W	-	0x01
0xD1	Bit [3:0]	R_WOI1_Frame_Thd[12:8]	-	R/W	0	0x00
0xD3	-	R_WOI2_Frame_Thd[7:0]	-	R/W	-	0x01
0xD4	Bit [3:0]	R_WOI2_Frame_Thd[12:8]	-	R/W	0	0x00
0xD6	-	R_WOI3_Frame_Thd[7:0]	-	R/W	-	0x01
0xD7	Bit [3:0]	R_WOI3_Frame_Thd[12:8]	-	R/W	0	0x00
0xD9	-	R_WOI4_Frame_Thd[7:0]	-	R/W	-	0x01
0xDA	Bit [3:0]	R_WOI4_Frame_Thd[12:8]	-	R/W	0	0x00

Table 34. Bank1 Registers

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0xC2	-	R_WOI_HSize[7:0]	◎	R/W	-	0x00
0xC3	Bit [1:0]	R_WOI_HSize[9:8]	◎	R/W	0	0x00
0xCB	-	R_WOI_VSize[7:0]	◎	R/W	-	0x04
0xCC	Bit [0]	R_WOI_VSize[8]	◎	R/W	0	0x00
0xCE	-	R_WOI_HStart[7:0]	◎	R/W	-	0x00

Table 35. Bank2 Registers

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0x21	-	R_WOI_HSize[7:0]	◎	R/W	-	0x40
0x22	Bit [1:0]	R_WOI_HSize[9:8]	◎	R/W	1	0x01
0x23	-	R_WOI_VSize[7:0]	◎	R/W	-	0xF0
0x24	Bit [0]	R_WOI_VSize[8]	◎	R/W	0	0x00
0x25	-	R_WOI_HStart[7:0]	◎	R/W	-	0x00
0x26	Bit [1:0]	R_WOI_HStart[9:8]	◎	R/W	0	0x00
0x27	-	R_WOI_VStart[7:0]	◎	R/W	-	0x0C
0x28	Bit [0]	R_WOI_VStart[8]	◎	R/W	0	0x00
0x55	Bit [0]	R_WOI_EnH	◎	R/W	1	0x01
0x79	Bit [1:0]	R_expo_LED_Manual_Mode_Sel[1:0]	-	R/W	0	0x00
0x7A	Bit [3:0]	R_expo_LED_Period[3:0]	-	R/W	0	0x00
0x7B	-	R_expo_LED_early[7:0]	-	R/W	-	0x01
0x7C	Bit [0]	R_expo_LED_polarity	-	R/W	0	0x00
0xC1	-	R_LineTime[7:0]	-	R/W	-	0x6C
0xC2	Bit [5:0]	R_LineTime[13:8]	-	R/W	7	0x07

Table 36. Bank4 Registers

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0x30	-	AE Enable Control	-	R/W	-	0x10
	Bit [1]	R_AE_manual_En	-		0	
	Bit [0]	R_AE_EnH	-		0	
0x31	-	R_Ytar8bit[7:0]	-	R/W	-	0x80
0x32	-	R_AE_LockRange_In[7:0]	-	R/W	-	0x08
0x33	-	R_AE_LockRange_Out_LB[7:0]	-	R/W	-	0x10
0x34	-	R_AE_LockRange_Out_UB[7:0]	-	R/W	-	0x10
0x38	-	R_AE_Start_div4_X[7:0]	-	R/W	-	0x00

Address	Bit Field	Name	Register Update	Access	Bit Field Default Value	Default Value
0x39	-	R_AE_Start_div4_Y[7:0]	-	R/W	-	0x00
0x3A	-	R_AE_Size__div4_X[7:0]	-	R/W	-	0x50
0x3B	-	R_AE_Size__div4_Y[7:0]	-	R/W	-	0x3C
0x40	-	R_AE_MinGain[7:0]	-	R/W	-	0x30
0x41	Bit [2:0]	R_AE_MinGain[10:8]	-	R/W	0	0x00
0x42	-	R_AE_MaxGain[7:0]	-	R/W	-	0x00
0x43	Bit [2:0]	R_AE_MaxGain[10:8]	-	R/W	1	0x01
0x44	-	R_AE_MinExpo[7:0]	-	R/W	-	0xC8
0x45	-	R_AE_MinExpo[15:8]	-	R/W	-	0x00
0x46	-	R_AE_MinExpo[23:16]	-	R/W	-	0x00
0x47	Bit [3:0]	R_AE_MinExpo[27:24]	-	R/W	0	0x00
0x48	-	R_AE_MaxExpo[7:0]	-	R/W	-	0x80
0x49	-	R_AE_MaxExpo[15:8]	-	R/W	-	0x1A
0x4A	-	R_AE_MaxExpo[23:16]	-	R/W	-	0x06
0x4B	Bit [3:0]	R_AE_MaxExpo[27:24]	-	R/W	0	0x00
0x51	-	R_AE_Gain_manual[7:0]	◎	R/W	-	0x00
0x52	Bit [2:0]	R_AE_Gain_manual[10:8]	◎	R/W	1	0x01
0x53	-	R_AE_Expo_manual[7:0]	◎	R/W	-	0x04
0x54	-	R_AE_Expo_manual[15:8]	◎	R/W	-	0x29
0x55	-	R_AE_Expo_manual[23:16]	◎	R/W	-	0x00
0x56	Bit [3:0]	R_AE_Expo_manual[27:24]	◎	R/W	0	0x00
0xA5	-	AE_Total_Gain[7:0]	-	R	-	-
0xA6	Bit [2:0]	AE_Total_Gain[10:8]	-	R	-	-
0xA7	-	Reg_ExpPxclkNum[7:0]	-	R	-	-
0xA8	-	Reg_ExpPxclkNum[15:8]	-	R	-	-
0xA9	-	Reg_ExpPxclkNum[23:16]	-	R	-	-
0xAA	Bit [3:0]	Reg_ExpPxclkNum[27:24]	-	R	-	-
0xD0	-	Multi-sensor control	-	R/W	-	0x00
	Bit [5:4]	R_Fsync_SlaveNum[1:0]	-		0	
	Bit [2]	R_Fsync_SlaveLabel	-		0	
	Bit [1]	R_Fsync_Master	-		0	
	Bit [0]	R_Fsync_En	-		0	
0xD1	Bit [3:0]	R_Fsync_Output_HoldTime[3:0]	-	R/W	10	0x0A
0xD2	-	R_Fsync_O_dly1[7:0]	-	R/W	-	0x00
0xD3	-	R_Fsync_O_dly1[15:8]	-	R/W	-	0x00
0xD4	-	R_Fsync_O_dly2[7:0]	-	R/W	-	0x00
0xD5	-	R_Fsync_O_dly2[15:8]	-	R/W	-	0x00

11.2 Register Description

Register Name	External Clock Function 1		
Bank	0x00	**Address**	0x26
Access	R/W	**Default Value**	0x0A
Bit Field	**Name**	**Default Value**	**Description**
6:4	T_spll_predivider[8:6]	0	Bit[8:6] of T_spll_predivider[8:0]
Register Name	**External Clock Function 1**		
Bank	0x00	**Address**	0x27
Access	R/W	**Default Value**	0x41
Bit Field	**Name**	**Default Value**	**Description**
5:0	T_spll_predivider[5:0]	1	Bit[5:0] of T_spll_predivider[8:0]
Description	Control Register for External Clock. For external clock modified. Refer to Section 5.5.3.		

Register Name	External Clock Function 2		
Bank	0x00	**Address**	0x29
Access	R/W	**Default Value**	0x64
Bit Field	**Name**	**Default Value**	**Description**
5:0	T_spll_postdivider[5:0]	36	Bit[5:0] of T_spll_postdivider[8:0]
Register Name	**External Clock Function 2**		
Bank	0x00	**Address**	0x2A
Access	R/W	**Default Value**	0x10
Bit Field	**Name**	**Default Value**	**Description**
6:4	T_spll_postdivider[8:6]	1	Bit[8:6] of T_spll_postdivider[8:0]
Description	Control Register for External Clock		

Register Name	External Clock Function 3		
Bank	0x00	**Address**	0x2B
Access	R/W	**Default Value**	0x03
Description	Control Register for External Clock		
Bit Field	**Name**	**Default Value**	**Description**
1	T_spll_refsel	1	0: Using external clock 1: Using internal clock
0	T_spll_clock	1	0: Using external clock 1: Using internal clock

Register Name	External Clock Function 4		
Bank	0x00	**Address**	0x36
Access	R/W	**Default Value**	0x02
Description	Control Register for External Clock		
Bit Field	**Name**	**Default Value**	**Description**
1:0	B_spll_EnH	2	0: Using external clock 2: Using internal clock

Register Name	R_LineTime [7:0]		
Bank	0x02	**Address**	0xC1
Access	R/W	**Default Value**	0x6C
Register Name	**R_LineTime [13:8]**		
Bank	0x02	**Address**	0xC2
Access	R/W	**Default Value**	0x07
Bit Field	**Name**	**Default Value**	**Description**
5:0	R_LineTime [13:8]	7	Bit[13:8] of R_LineTime [13:0]
Description	The Line Time Register		

Register Name	Part ID[7:0]		
Bank	0x00	**Address**	0x00
Access	R	**Default Value**	0x20
Register Name	**Part ID[15:8]**		
Bank	0x00	**Address**	0x01
Access	R	**Default Value**	0x79
Description	Part ID of the sensor		

Register Name	Bank_Number		
Bank	0x00	**Address**	0xEF
Access	W	**Default Value**	0x00
Description	Register Bank Number. Configure to Switch Register Bank.		

Register Name	Update Flag		
Bank	0x00	**Address**	0xEB
Access	R/W	**Default Value**	0x80
Bit Field	**Name**	**Default Value**	**Description**
7	Update flag	1	Update flag= 1 to official the activation.

Register Name	R_Trigger_FrameNum		
Bank	0x00	**Address**	0x2E
Access	R/W	**Default Value**	0x01
Description	Number of output frames for trigger mode.		

Register Name	R_TG_En		
Bank	0x00	**Address**	0x30
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	R_TG_En	0	0: Suspend state. 1: Operation state.

Register Name	R_Trigger_En		
Bank	0x00	Address	0x31
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
0	R_Trigger_En	0	0: Exit Trigger mode 1: Enter Trigger mode

Register Name	R_WOI_Enable		
Bank	0x00	Address	0x80
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
3	R_WOI_En1	0	0: disable first motion window 1: enable first motion window
2	R_WOI_En2	0	0: disable second motion window 1: enable second motion window
1	R_WOI_En3	0	0: disable third motion window 1: enable third motion window
0	R_WOI_En4	0	0: disable fourth motion window 1: enable fourth motion window

Register Name	R_WOI_detect_Zone		
Bank	0x00	Address	0x81
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
3	R_WOI_InorEx1	0	0: detect motion inner of 1st motion window zone 1: detect motion outer of 1st motion window zone
2	R_WOI_InorEx2	0	0: detect motion inner of 2nd motion window zone 1: detect motion outer of 2nd window zone
1	R_WOI_InorEx3	0	0: detect motion inner of 3rd motion window zone 1: detect motion outer of 3rd motion window zone
0	R_WOI_InorEx4	0	0: detect motion inner of 4th motion window zone 1: detect motion outer of 4th motion window zone

Register Name	R_WOI_VStart1[5:0]		
Bank	0x00	Address	0x82
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VStart1[5:0]	0	Vertical start position of motion WOI1.

Register Name	R_WOI_HStart1[6:0]		
Bank	0x00	Address	0x83
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HStart1[6:0]	0	Horizontal start position of motion WOI1.

Register Name	R_WOI_VEnd1[5:0]		
Bank	0x00	Address	0x84
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VEnd1[5:0]	0	Vertical end position of motion WOI1.

Register Name	R_WOI_HEnd1[6:0]		
Bank	0x00	Address	0x85
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HEnd1[6:0]	0	Horizontal end position of motion WOI1.

Register Name	R_WOI_VStart2[5:0]		
Bank	0x00	Address	0x86
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VStart2[5:0]	0	Vertical start position of motion WOI2.

Register Name	R_WOI_HStart2[6:0]		
Bank	0x00	Address	0x87
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HStart2[6:0]	0	Horizontal start position of motion WOI2.

Register Name	R_WOI_VEnd2[5:0]		
Bank	0x00	Address	0x88
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VEnd2[5:0]	0	Vertical end position of motion WOI2.

Register Name	R_WOI_HEnd2[6:0]		
Bank	0x00	Address	0x89
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HEnd2[6:0]	0	Horizontal end position of motion WOI2.

Register Name	R_WOI_VStart3[5:0]		
Bank	0x00	Address	0x8A
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VStart3[5:0]	0	Vertical start position of motion WOI3.

Register Name	R_WOI_HStart3[6:0]		
Bank	0x00	Address	0x8B
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HStart3[6:0]	0	Horizontal start position of motion WOI3.

Register Name	R_WOI_VEnd3[5:0]		
Bank	0x00	Address	0x8C
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VEnd3[5:0]	0	Vertical end position of motion WOI3.

Register Name	R_WOI_HEnd3[6:0]		
Bank	0x00	Address	0x8D
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HEnd3[6:0]	0	Horizontal end position of motion WOI3.

Register Name	R_WOI_VStart4[5:0]		
Bank	0x00	Address	0x8E
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VStart4[5:0]	0	Vertical start position of motion WOI4.

Register Name	R_WOI_HStart4[6:0]		
Bank	0x00	Address	0x8F
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
6:0	R_WOI_HStart4[6:0]	0	Horizontal start position of motion WOI4.

Register Name	R_WOI_VEnd4[5:0]		
Bank	0x00	Address	0x90
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
5:0	R_WOI_VEnd4[5:0]	0	Vertical end position of motion WOI4.

Register Name	R_WOI_HEnd4[6:0]		
Bank	0x00	**Address**	0x91
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
6:0	R_WOI_HEnd4[6:0]	0	Horizontal end position of motion WOI4.

Register Name	WOIn_Motion		
Bank	0x00	**Address**	0x94
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
3	WOI1_Motion	0	1: motion event is triggered of first WOI
2	WOI2_Motion	0	1: motion event is triggered of second WOI
1	WOI3_Motion	0	1: motion event is triggered of third WOI
0	WOI4_Motion	0	1: motion event is triggered of fourth WOI

Register Name	WOI1_Diff_cnt[7:0]		
Bank	0x00	**Address**	0x97
Access	R	**Default Value**	0x00
Register Name	**WOI1_Diff_cnt[12:8]**		
Bank	0x00	**Address**	0x98
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
4:0	WOI1_Diff_cnt[12:8]	0	Bit[12:8] of WOI1_Diff_cnt[12:0]
Description	Motion pixels counter		

Register Name	WOI2_Diff_cnt[7:0]		
Bank	0x00	Address	0x99
Access	R	Default Value	0x00
Register Name	WOI2_Diff_cnt[12:8]		
Bank	0x00	Address	0x9A
Access	R	Default Value	0x00
Bit Field	Name	Default Value	Description
4:0	WOI2_Diff_cnt[12:8]	0	Bit[12:8] of WOI2_Diff_cnt[12:0]
Description	Motion pixels counter		

Register Name	WOI3_Diff_cnt[7:0]		
Bank	0x00	Address	0x9B
Access	R	Default Value	0x00
Register Name	WOI3_Diff_cnt[12:8]		
Bank	0x00	Address	0x9C
Access	R	Default Value	0x00
Bit Field	Name	Default Value	Description
4:0	WOI3_Diff_cnt[12:8]	0	Bit[12:8] of WOI3_Diff_cnt[12:0]
Description	Motion pixels counter		

Register Name	WOI4_Diff_cnt[7:0]		
Bank	0x00	Address	0x9D
Access	R	Default Value	0x00
Register Name	WOI4_Diff_cnt[12:8]		
Bank	0x00	Address	0x9E
Access	R	Default Value	0x00
Bit Field	Name	Default Value	Description
4:0	WOI4_Diff_cnt[12:8]	0	Bit[12:8] of WOI4_Diff_cnt[12:0]
Description	Motion pixels counter		

Register Name	Frame_Diff_Pixel_Xmin[6:0]		
Bank	0x00	**Address**	0x9F
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
6:0	Frame_Diff_Pixel_Xmin[6:0]	0	X start position of Motion pixels area

Register Name	Frame_Diff_Pixel_Xmax[6:0]		
Bank	0x00	**Address**	0xA0
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
6:0	Frame_Diff_Pixel_Xmax[6:0]	0	X end position of Motion pixels area

Register Name	Frame_Diff_Pixel_Ymin[5:0]		
Bank	0x00	**Address**	0xA1
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
5:0	Frame_Diff_Pixel_Ymin[5:0]	0	Y start position of Motion pixels area

Register Name	Frame_Diff_Pixel_Ymax[5:0]		
Bank	0x00	**Address**	0xA2
Access	R	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
5:0	Frame_Diff_Pixel_Ymax[5:0]	0	Y end position of Motion pixels area

- Parallel Interface Register

Register Name	Parallel Interface Polarity		
Bank	0x00	**Address**	0xAF
Access	R/W	**Default Value**	0x31
Description	Set parallel interface clock active level and data output type		
Bit Field	**Name**	**Default Value**	**Description**
6	R_Parallel_Pxclk_Inv	0	0: Configure sensor to output data at falling edge and the host latches data at rising edge. 1: Configure sensor to output data at rising edge and the host latches data at falling edge.
5	R_Parallel_Hsync_Inv	0	0: Configure to active low 1: Configure to active high
4	R_Parallel_Vsync_Inv	0	0: Configure to active low 1: Configure to active high

Register Name	R_WOI1_Frame_Thd[7:0]		
Bank	0x00	**Address**	0xD0
Access	R/W	**Default Value**	0x01
Register Name	**R_WOI1_Frame_Thd[12:8]**		
Bank	0x00	**Address**	0xD1
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
4:0	R_WOI1_Frame_Thd[12:8]	0	Bit [12:8] of R_WOI1_Frame_Thd[12:0]
Description	Total number motion pixels threshold of motion event.		

Register Name	R_WOI2_Frame_Thd[7:0]		
Bank	0x00	**Address**	0xD3
Access	R/W	**Default Value**	0x01
Register Name	**R_WOI2_Frame_Thd[12:8]**		
Bank	0x00	**Address**	0xD4
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
4:0	R_WOI2_Frame_Thd[12:8]	0	Bit [12:8] of R_WOI2_Frame_Thd[12:0]
Description	Total number motion pixels threshold of motion event.		

Register Name	R_WOI3_Frame_Thd[7:0]		
Bank	0x00	**Address**	0xD6
Access	R/W	**Default Value**	0x01
Register Name	**R_WOI3_Frame_Thd[12:8]**		
Bank	0x00	**Address**	0xD7
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
4:0	R_WOI3_Frame_Thd[12:8]	0	Bit [12:8] of R_WOI3_Frame_Thd[12:0]
Description	Total number motion pixels threshold of motion event.		

Register Name	R_WOI4_Frame_Thd[7:0]		
Bank	0x00	**Address**	0xD9
Access	R/W	**Default Value**	0x01
Register Name	**R_WOI4_Frame_Thd[12:8]**		
Bank	0x00	**Address**	0xDA
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
4:0	R_WOI4_Frame_Thd[12:8]	0	Bit [12:8] of R_WOI4_Frame_Thd[12:0]
Description	Total number motion pixels threshold of motion event.		

Register Name	IntFlag_1[3:0]		
Bank	0x00	**Address**	0x04
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
3:0	IntFlag_1[3:0]	0	Interrupt status. 1: It means the INT event happen bit[0]: Motion_INT_WOI4 bit[1]: Motion_INT_WOI3 bit[2]: Motion_INT_WOI2 bit[3]: Motion_INT_WOI1

Register Name	R_IntFlag_1_RdClr_En		
Bank	0x00	**Address**	0x05
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	R_IntFlag_1_RdClr_En	0	0: Non-clear Interrupt flag register value after host read 1: Clear Interrupt flag register value after host read

Register Name	Rs_MotionDetection_EnH		
Bank	0x00	**Address**	0x79
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	Rs_MotionDetection_EnH	0	0: disable motion detection 1: enable motion detection.

Register Name	R_Int_1_En[3:0]		
Bank	0x00	**Address**	0xA4
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
3:0	R_Int_1_En[3:0]	0	Motion interrupt enable bits. bit[0]: Motion_INT_WOI4 bit[1]: Motion_INT_WOI3 bit[2]: Motion_INT_WOI2 bit[3]: Motion_INT_WOI1

Register Name	R_Int_Inv		
Bank	0x00	**Address**	0xA6
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	R_Int_Inv	0	Configure the polarity of INT pin. Below shows the default value in different modes, ▪ Motion Mode: 0: Low Active; 1: High Active. ▪ Interrupt for SPI Image Output Mode: 0: High Active; 1: Low Active

Register Name	R_GPIO1_sel[7:0]		
Bank	0x00	**Address**	0x07
Access	R/W	**Default Value**	0x00
Description	GPIO1 output selection 0: set to output signal 1: set to external LED control signal 2: set to motion mode interrupt signal 3: set to frame synchronization signal 4: set to SPI image output interrupt signal		

Register Name	R_GPIO2_sel[7:0]		
Bank	0x00	**Address**	0x08
Access	R/W	**Default Value**	0x00
Description	GPIO2 output selection 0: set to output signal		

Register Name	GPIO control		
Bank	0x00	**Address**	0x0D
Access	R/W	**Default Value**	0x00
Description	GPIO input and output data.		

Bit Field	Name	Default Value	Description
5	AD_GPIO2	0	GPIO2 input data. (read-only) 0: low, 1: high
4	AD_GPIO1	0	GPIO1 input data. (read-only) 0: low, 1: high
1	R_GPIO2_O	0	GPIO2 output data. 0: low, 1: high
0	R_GPIO1_O	0	GPIO1 output data. 0: low, 1: high

Register Name	GPIO1 control		
Bank	0x00	**Address**	0x0E
Access	R/W	**Default Value**	0x40
Description	GPIO1 input and output control.		

Bit Field	Name	Default Value	Description
7	T_GPIO1_OE	0	GPIO1 pads output buffer. 0: disable, 1: enable
6	T_GPIO1_INL	1	GPIO1 pads input buffer. 0: enable, 1: disable
5	T_GPIO1_IDDQ	0	GPIO1 pads IDDQ control.
4	T_GPIO1_SR	0	GPIO1 pads output slew rate control.
3:2	T_GPIO1_OPDRV [1:0]	0	GPIO1 pads output driving control.
1	T_GPIO1_PD	0	GPIO1 pads pull down resistor. 0: disable, 1: enable
0	T_GPIO1_PU	0	GPIO1 pads pull up resistor. 0: disable, 1: enable

Register Name	GPIO2 control		
Bank	0x00	**Address**	0x0F
Access	R/W	**Default Value**	0x40
Description	GPIO2 input and output control.		

Bit Field	Name	Default Value	Description
7	T_GPIO2_OE	0	GPIO2 pads output buffer. 0: disable, 1: enable
6	T_GPIO2_INL	1	GPIO2 pads input buffer. 0: enable, 1: disable
5	T_GPIO2_IDDQ	0	GPIO2 pads IDDQ control.
4	T_GPIO2_SR	0	GPIO2 pads output slew rate control.
3:2	T_GPIO2_OPDRV [1:0]	0	GPIO2 pads output driving control.
1	T_GPIO2_PD	0	GPIO2 pads pull down resistor. 0: disable, 1: enable
0	T_GPIO2_PU	0	GPIO2 pads pull up resistor. 0: disable 1: enable

Register Name	R_expo_LED_Manual_Mode_Sel [1:0]		
Bank	0x02	**Address**	0x79
Access	R/W	**Default Value**	0x00
Description	LED control signal auto/manual control.		

Bit Field	Name	Default Value	Description
1:0	R_expo_LED_Manual_Mode_Sel	0	0: auto toggle 1: always on 2: always off

Register Name	R_expo_LED_Period [3:0]		
Bank	0x02	**Address**	0x7A
Access	R/W	**Default Value**	0x00
Description	LED control signal period.		

Bit Field	Name	Default Value	Description
3:0	R_expo_LED_Period	0	0: every frame output 1: two frames output once 2: three frames output once, and so on.

Register Name	R_expo_LED_early [7:0]		
Bank	0x02	**Address**	0x7B
Access	R/W	**Default Value**	0x01
Description	Amount of delay time between LED start and exposure state. Unit: about (1/32000) sec.		

Register Name	R_expo_LED_polarity		
Bank	0x02	**Address**	0x7C
Access	R/W	**Default Value**	0x00
Description	LED polarity control		

Bit Field	Name	Default Value	Description
0	R_expo_LED_polarity	0	0: active Low 1: active high

Register Name	Multi-sensor control		
Bank	0x04	**Address**	0xD0
Access	R/W	**Default Value**	0x00
Description	Multi-sensor control registers		

Bit Field	Name	Default Value	Description
5:4	R_Fsync_SlaveNum	0	Number of slave numbers. 1: 1 slave. (2-sensor mode) 2: 2 slaves. (3-sensor mode)
2	R_Fsync_SlaveLabel	0	FSYNC slave label select. 0: Slave1. 1: Slave2.
1	R_Fsync_Master	0	FSYNC mode select. 0: FSYNC slave mode. 1: FSYMC master mode.
0	R_Fsync_En	0	FSYNC mode enable.

Register Name	R_Fsync_Output_HoldTime[3:0]		
Bank	0x04	**Address**	0xD1
Access	R/W	**Default Value**	0x0A
Description	FSYNC I/O timing control		

Bit Field	Name	Default Value	Description
3:0	R_Fsync_Output_HoldTime	10	FSYNC I/O timing control.

Register Name	R_Fsync_O_dly1[7:0]		
Bank	0x04	**Address**	0xD2
Access	R/W	**Default Value**	0x00
Register Name	**R_Fsync_O_dly1[15:8]**		
Bank	0x04	**Address**	0xD3
Access	R/W	**Default Value**	0x00
Description	For FSYNC master only. FSYNC pin timing control		

Register Name	R_Fsync_O_dly2[7:0]		
Bank	0x04	**Address**	0xD4
Access	R/W	**Default Value**	0x00
Register Name	**R_Fsync_O_dly2[15:8]**		
Bank	0x04	**Address**	0xD5
Access	R/W	**Default Value**	0x00
Description	FSYNC pin timing control. For FSYNC master only		

Register Name	R_Frame_Time[7:0]		
Bank	0x00	**Address**	0x4C
Access	R/W	**Default Value**	0x40
Register Name	**R_Frame_Time[15:8]**		
Bank	0x00	**Address**	0x4D
Access	R/W	**Default Value**	0x0D
Register Name	**R_Frame_Time[23:16]**		
Bank	0x00	**Address**	0x4E
Access	R/W	**Default Value**	0x03
Register Name	**R_Frame_Time[27:24]**		
Bank	0x00	**Address**	0x4F
Access	R/W	**Default Value**	0x00

Bit Field	Name	Default Value	Description
3:0	R_Frame_Time[27:24]	0	Bit [27:24] of R_Frame_Time[27:0]
Description	Adjust Frame rate		

Register Name	R_Normal_PwrSv[0]		
Bank	0x00	**Address**	0x55
Access	R/W	**Default Value**	0x01

Bit Field	Name	Default Value	Description
0	R_Normal_PwrSv[0]	0	Sensor normal power saving, 0: Frame rate ≥150fps 1: Frame rate <150fps

Register Name	R_AE_Start_div4_X		
Bank	0x04	**Address**	0x38
Access	R/W	**Default Value**	0x00
Description	AE window X start position		

Register Name	R_AE_Start_div4_Y		
Bank	0x04	**Address**	0x39
Access	R/W	**Default Value**	0x00
Description	AE window Y start position		

Register Name	R_AE_Size_div4_X		
Bank	0x04	**Address**	0x3A
Access	R/W	**Default Value**	0x50
Description	AE sub-window, size (X)		

Register Name	R_AE_Size_div4_Y		
Bank	0x04	**Address**	0x3B
Access	R/W	**Default Value**	0X3C
Bit Field	**Name**	**Default Value**	**Description**
Description	AE sub-window, size (Y)		

Register Name	AE Enable Control		
Bank	0x04	**Address**	0x30
Access	R/W	**Default Value**	0x10
Description	AE enable control		
Bit Field	**Name**	**Default Value**	**Description**
1	R_AE_manual_En	0	Manual control exposure time and gain, 0: Disable. 1: Enable manual mode.
0	R_AE_EnH	0	Auto control exposure time and gain 0: AE/AG disable 1: AE/AG enable

Register Name	R_Ytar8bit (Ytarget)		
Bank	0x04	**Address**	0x31
Access	R/W	**Default Value**	0x80
Description	AE is converged base on setting target to a bright intensity.		

Register Name	R_AE_LockRange_In		
Bank	0x04	**Address**	0x32
Access	R/W	**Default Value**	0x08
Description	If AE window bright intensity was inside lock range, the exposure time and gain would stop to adjust.		

Register Name	R_AE_LockRange_Out_LB		
Bank	0x04	**Address**	0x33
Access	R/W	**Default Value**	0x10
Description	If AE window bright intensity smaller than *R_AE_LockRange_Out_LB*, the image bright intensity will be adjusted.		

Register Name	R_AE_LockRange_Out_UB		
Bank	0x04	**Address**	0x34
Access	R/W	**Default Value**	0x10
Description	If AE window bright intensity greater than *R_AE_LockRange_Out_UB*, the image bright intensity will be adjusted.		

Register Name	R_AE_MinExpo [7:0]		
Bank	0x04	Address	0x44
Access	R/W	Default Value	0xC8
Register Name	R_AE_MinExpo [15:8]		
Bank	0x04	Address	0x45
Access	R/W	Default Value	0x00
Register Name	R_AE_MinExpo [23:16]		
Bank	0x04	Address	0x46
Access	R/W	Default Value	0x00
Register Name	R_AE_MinExpo [27:24]		
Bank	0x04	Address	0x47
Access	R/W	Default Value	0x00

Bit Field	Name	Default Value	Description
3:0	R_AE_MinExpo [27:24]	0	Bit [27:24] of R_AE_MinExpo [27:0]
Description	Minimum exposure time value for auto exposure time control		

Register Name	R_AE_MaxExpo [7:0]		
Bank	0x04	Address	0x48
Access	R/W	Default Value	0x80
Register Name	R_AE_MaxExpo [15:8]		
Bank	0x04	Address	0x49
Access	R/W	Default Value	0x1A
Register Name	R_AE_MaxExpo [23:16]		
Bank	0x04	Address	0x4A
Access	R/W	Default Value	0x06
Register Name	R_AE_MaxExpo [27:24]		
Bank	0x04	Address	0x4B
Access	R/W	Default Value	0x00

Bit Field	Name	Default Value	Description
3:0	R_AE_MaxExpo [27:24]	0	Bit [27:24] of R_AE_MaxExpo [27:0]
Description	Maximum exposure time value for auto exposure time control		

Register Name	R_AE_MinGain [7:0]		
Bank	0x04	Address	0x40
Access	R/W	Default Value	0x30
Register Name	R_AE_MinGain [10:8]		
Bank	0x04	Address	0x41
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
2:0	R_AE_MinGain [10:8]	0	Bit [10:8] of R_AE_MinGain [10:0]
Description	Minimum gain value for auto gain control		

Register Name	R_AE_MaxGain [7:0]		
Bank	0x04	Address	0x42
Access	R/W	Default Value	0xD0
Register Name	R_AE_MaxGain [10:8]		
Bank	0x04	Address	0x43
Access	R/W	Default Value	0x01
Bit Field	Name	Default Value	Description
2:0	R_AE_MaxGain [10:8]	1	Bit[10:8] of R_AE_MaxGain [10:0]
Description	Maximum gain value for auto gain control		

Register Name	AE_Total_Gain[7:0]		
Bank	0x04	Address	0xA5
Access	R	Default Value	-
Register Name	AE_Total_Gain[10:8]		
Bank	0x04	Address	0xA6
Access	R	Default Value	-
Bit Field	Name	Default Value	Description
2:0	AE_Total_Gain[10:8]	n/a	Bit[10:8] of AE_Total_Gain[10:0]
Description	Analog gain value of the present image		

Register Name	Reg_ExpPxclkNum[7:0]		
Bank	0x04	Address	0xA7
Access	R	Default Value	-
Register Name	Reg_ExpPxclkNum[15:8]		
Bank	0x04	Address	0xA8
Access	R	Default Value	-
Register Name	Reg_ExpPxclkNum[23:16]		
Bank	0x04	Address	0xA9
Access	R	Default Value	-
Register Name	Reg_ExpPxclkNum[27:24]		
Bank	0x04	Address	0xAA
Access	R	Default Value	-

Bit Field	Name	Default Value	Description
3:0	Reg_ExpPxclkNum[27:24]	n/a	Bit[27:24] of Reg_ExpPxclkNum[27:0]
Description	Exposure time of the present image		

Register Name	R_AE_Gain_manual[7:0]		
Bank	0x04	Address	0x51
Access	R/W	Default Value	0x00
Register Name	R_AE_Gain_manual[10:8]		
Bank	0x04	Address	0x52
Access	R/W	Default Value	0x01

Bit Field	Name	Default Value	Description
2:0	R_AE_Gain_manual[10:8]	1	Bit [10:8] of R_AE_Gain_manual [10:0]
Description	Gain value for manual gain control		

Register Name	R_AE_Expo_manual [7:0]		
Bank	0x04	Address	0x53
Access	R/W	Default Value	0x04
Register Name	R_AE_Expo_manual [15:8]		
Bank	0x04	Address	0x54
Access	R/W	Default Value	0x29
Register Name	R_AE_Expo_manual [23:16]		
Bank	0x04	Address	0x55
Access	R/W	Default Value	0x00
Register Name	R_AE_Expo_manual [27:24]		
Bank	0x04	Address	0x56
Access	R/W	Default Value	0x00

Bit Field	Name	Default Value	Description
3:0	R_AE_MinExpo[27:24]	0	Bit [27:24] of R_AE_MinExpo [27:0]
Description	Exposure time value for manual exposure time control		

Register Name	Mirror		
Bank	0x00	Address	0x09
Access	R/W	Default Value	0x50
Description	Adjust image horizontal direction		

Bit Field	Name	Default Value	Description
4	R_HFlip2	1	*R_HFlip2*, perform horizontal flip function 0: horizontal flip 1: original image
1	R_HFlip1	0	*R_HFlip1*, perform horizontal flip function 0: original image 1: horizontal flip

Register Name	Flip		
Bank	0x01	**Address**	0xCE
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
2	R_VFlip	0	Adjust image vertical direction *R_VFlip*, perform vertical flip function 0: original image. 1: vertical flip

Register Name	R_VsettleStart [7:0]		
Bank	0x01	**Address**	0xC2
Access	R/W	**Default Value**	0x00
Register Name	**R_VsettleStart [8]**		
Bank	0x01	**Address**	0xC3
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	R_VsettleStart [8]	0	Bit[8] of R_VsettleStart [8:0]
Description	Line dummy address of image. If vertical flip function is used, the register value set to 247.		

Register Name	R_VStart [7:0]		
Bank	0x01	**Address**	0xCB
Access	R/W	**Default Value**	0x04
Register Name	**R_VStart [8]**		
Bank	0x01	**Address**	0xCC
Access	R/W	**Default Value**	0x00
Bit Field	**Name**	**Default Value**	**Description**
0	R_VStart [8]	0	Bit[8] of R_VStart [8:0]
Description	Line start address of image. If vertical flip function is used, the register value set to 243		

Register Name	R_WOI_EnH		
Bank	0x02	Address	0x55
Access	R/W	Default Value	0x01
Bit Field	Name	Default Value	Description
0	R_WOI_EnH	1	WOI Function enable 0: Disable 1: Enable

Register Name	R_WOI_HSize[7:0]		
Bank	0x02	Address	0X21
Access	R/W	Default Value	0x40
Register Name	R_WOI_HSize[9:8]		
Bank	0x02	Address	0X22
Access	R/W	Default Value	0x01
Bit Field	Name	Default Value	Description
1:0	R_WOI_HSize[9:8]	1	Bit[9:8] of R_WOI_HSize[9:0]
Description	Horizontal of size of WOI.		

Register Name	R_WOI_VSize[7:0]		
Bank	0x02	Address	0X23
Access	R/W	Default Value	0xF0
Register Name	R_WOI_VSize[8]		
Bank	0x02	Address	0X24
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
0	R_WOI_VSize[8]	0	Bit[8] of R_WOI_VSize[8:0]
Description	Vertical of size of WOI.		

Register Name	R_WOI_HStart[7:0]		
Bank	0x02	Address	0x25
Access	R/W	Default Value	0x00
Register Name	R_WOI_HStart[9:8]		
Bank	0x02	Address	0x26
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
1:0	R_WOI_HStart[9:8]	0	Bit[9:8] of R_WOI_HStart[9:0]
Description	Horizontal of start position of WOI		

Register Name	R_WOI_VStart[7:0]		
Bank	0x02	Address	0x27
Access	R/W	Default Value	0x0C
Register Name	R_WOI_VStart[8]		
Bank	0x02	Address	0x28
Access	R/W	Default Value	0x00
Bit Field	Name	Default Value	Description
0	R_WOI_VStart[8]	0	Bit[8] of R_WOI_VStart[8:0]
Description	Vertical of start position of WOI. The value (12) is original point.		

Revision History

Revision Number	Date	Description
0.52	17 Nov 2025	Initial release version.
0.8	4 May 2026	Removed TBD items and finalized document.

Disclaimers

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